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Self-Selective Multi-Terminal Memtransistor Crossbar Array for In-Memory Computing

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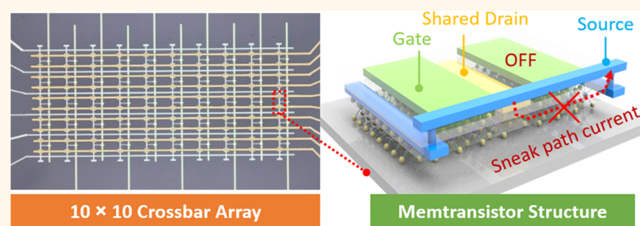
ABSTRACT: **Two-terminal resistive switching devices are commonly plagued with longstanding scientific issues including interdevice variability and sneak current that lead to computational errors and high-power consumption. This necessitates the integration of a separate selector in a one-transistor-one-RRAM (1T-1R) configuration to mitigate crosstalk issue, which compromises circuit footprint. Here, we demonstrate a multi-terminal memtransistor crossbar array with increased parallelism in programming *via* independent gate control, which allows *in situ* computation at a dense cell size of 3−4.5 F^2 and a minimal sneak current of 0.1 nA. Moreover, a low switching energy of 20 fJ/bit is achieved at a voltage of merely 0.42 V. The architecture is capable of performing multiply-and-accumulate operation, a core computing task for pattern classification. A high MNIST recognition accuracy of 96.87% is simulated owing to the linear synaptic plasticity. Such computing paradigm is deemed revolutionary toward enabling data-centric applications in artificial intelligence and Internet-of-things.**



KEYWORDS: *memtransistor, MoS_2, self-selective, multi-terminal, in-memory computing*

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The application of artificial intelligence (AI) technology in perception tasks (e.g., computer vision, speech recognition) and Internet-of-Things (IoT) puts significant demands on computing speed and power efficiency. However, conventional von Neumann architecture which physically separates the processing and memory units is suffering from fundamental limitation in data rate and energy consumption due to the enormous data movement between both subsystems. To overcome the memory wall and to push the envelope for energy efficiency, a radically different computing paradigm that allows in situ computation within the memory, or in-memory computing, is essential to address the issues associated with data-abundant computing driven by AI. For instance, in realizing artificial neural networks to perform image classification workloads, various types of crossbar array are constructed using nonvolatile memory (NVMs) such as two-terminal resistive random access memory (RRAM),[1,2] phase change memory (PCM)[3] or three-terminal flash memory,[4] ferroelectric field-effect transistors (FeFET),[5,6] among others.

Among the above-mentioned crossbar array architecture, the 1-R is the simplest form wherein a two-terminal RRAM is sandwiched between bit lines (BLs) and word lines (WLs), which provides excellent area efficiency (4 F^2) and very high-density integration.[1,2,7] However, the high sneak current that flows through the neighboring memory cells remains a fundamental issue. Such issue may be mitigated with a high $I-V$ nonlinearity by engineering the memristor itself[8−10] or by adding a rectifying selector to each cell (1S-1R).[11] However, the available array size is still limited since the performance requirement for memristor and selector is very demanding.[7] To further reduce sneak current and enable accurate programming/reading in large-scale crossbar array, the one-transistor one-resistor (1T-1R) architecture has been the most widely studied strategy wherein a selector transistor is integrated to each cell.[1,7] The third-terminal (gate) in the transistor offers better controllability even though this structure suffers from large circuit overhead (e.g., area, power)[7,12] and complex fabrication processes which detrimentally compromise the integration density. Therefore, three-terminal unit cell is desirable due to its ability to combine resistive switching (RS) and selection function into a single device without any footprint penalty. Some three-terminal unit cells, such as flash memory[4] and FeFET,[5,6] have been

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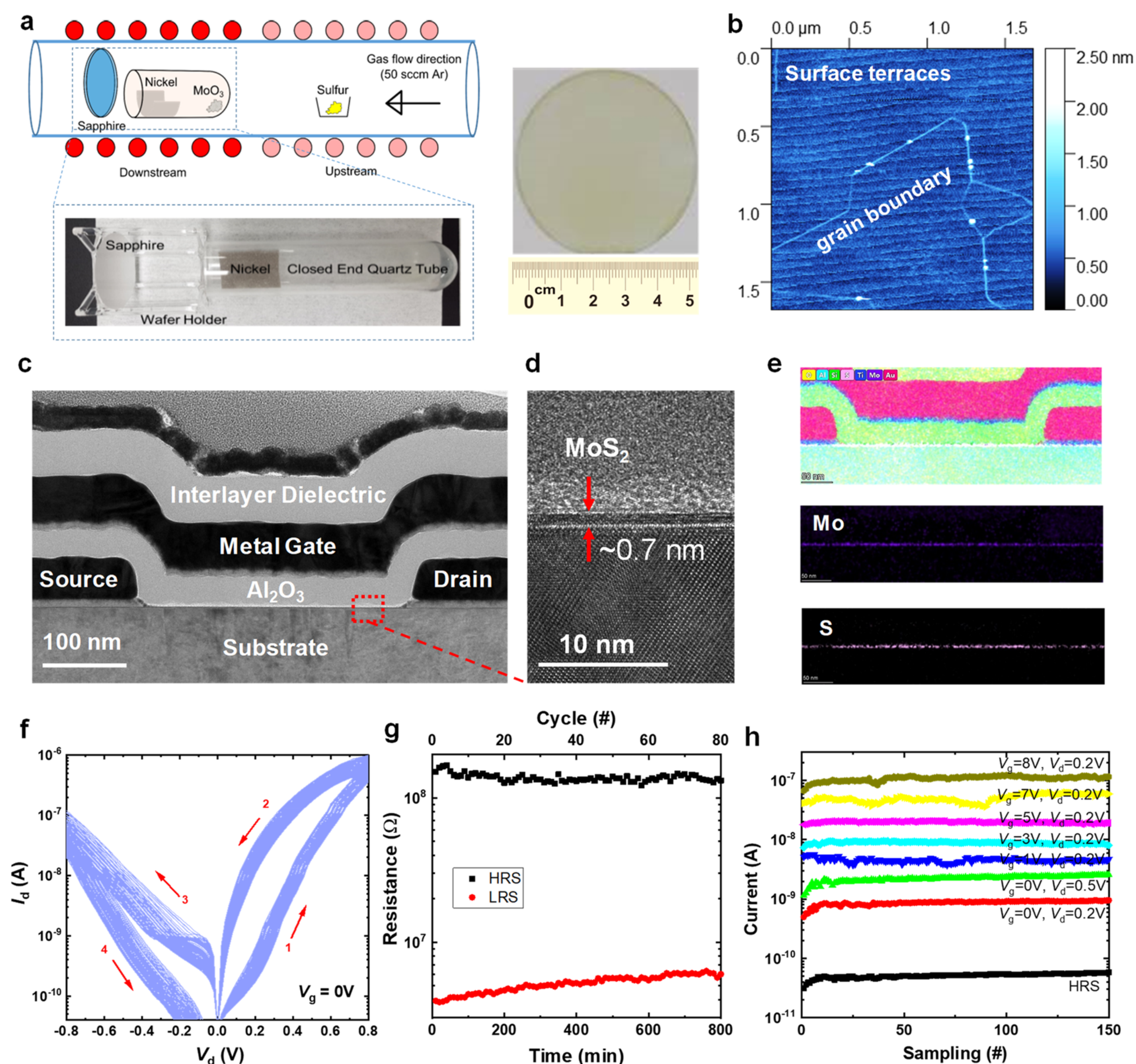

Figure 1. The structure and electrical performance of MoS_2memtransistor cell. (a) An illustration of the arrangement of substrate, crucible, and precursor flow placements in tube furnace for MoS_2 growth with sulfur (S) and MoO_3 in the upstream and downstream regions, respectively. The method enables 2 in. wafer-scale growth. (b) AFM scan image reveals the terraces due to annealed sapphire substrate steps and distinct grain boundaries within the grown MoS_2 film. (c) Cross-sectional TEM image of the memtransistor cell, showing a basic top-gated FET and the interlayer dielectric for source line interconnection. (d) Zoom-in view of the MoS_2 channel region indicated by the red dashed box, revealing the monolayer signature of MoS_2 channel material, with a scale bar of 10 nm. (e) EDS maps of the cross-section in (c) and the MoS_2 channel, respectively. (f) 150 cycles of $I_{ds}-V_{ds}$ curves of one single memtransistor cell measured at a grounded gate voltage. The red arrows indicate V_{ds} sweep direction, implying a nonvolatile RS behavior. (g) Retention behavior of the HRS and LRS for a duration of 800 min. The LRS is set by a 1 V DC loop. (h) Eight data storage levels are achieved with both the gate and drain terminals modulation.

investigated which are found to achieve a more linear and symmetric electrostatic gate control. However, the nonvolatile RS behavior is represented by the device threshold voltage and subsequent drain current modulation is achieved by gate voltage induced charge-trapping or ferroelectric polarization. Thus, despite being a three-terminal device, the gate control is still not able to provide additional selection function to avoid crosstalk issue in neighboring cells.

Memtransistor, a hybrid integration of memristor and transistor, could combine RS and selection functions into a single device structure.[13,14] Recently, multi-terminal memtransistors have been developed using chemical vapor deposition (CVD) grown single-layer polycrystalline molybdenum disulfide (MoS_2) thin film.[13,14] The memtransisor is configured in a field-effect transistor (FET) structure wherein the RS behavior is mainly programmed by drain voltage based on grain-boundary-mediated defects migration, whereas the gate terminal offers controllability over sneak current by turning off unselected cells. Moreover, the MoS_2 memtransistor is capable of implementing synaptic plasticity, making it a potential building block to realize artificial neural network (ANN) for in-memory computing.[13,14] Recently, a dual-gate memtransistor crossbar array is demonstrated with top- and bottom-gate to independently control each memtransistor.[15] To program individual memtransistor, a drain voltage of 20 V is applied to selected bit line at a global back-gate voltage of

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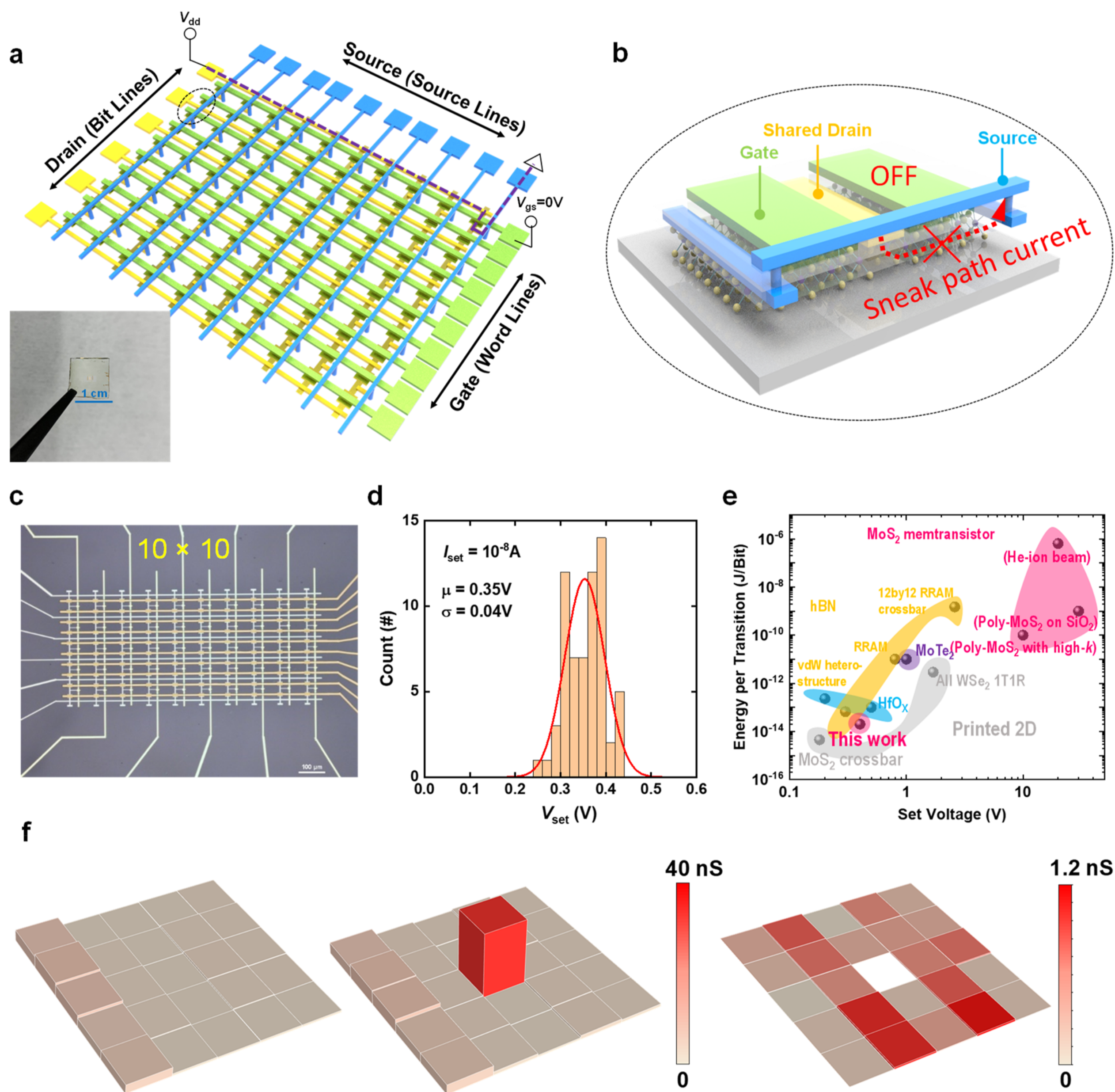

Figure 2. Electrical characterization of the MoS_2memtransistor crossbar array. (a) 3D schematic illustration of a 10 × 10 MoS_2 memtransistor crossbar array. Current flow paths through the selected cell during the write operation is indicated by a purple dashed line. The picture at the bottom left corner shows the as-fabricated crossbar array on sapphire substrate. (b) Zoom-in 3D schematic illustration of two neighboring memtransistor cells. The two cells have an individual gate terminal while sharing the same drain and source. (c) Top-view optical image of the as-fabricated MoS_2 memtransistor crossbar array. The horizontal drain (left) and gate (right) electrodes are the alternating bit lines and word lines, and the vertical electrodes are the source lines. (d) Histogram of the switching voltage at a set voltage of 10^{-8}A of 64 memtransistor cells. (e) Benchmark plot comparing the switching energy per bit vs. switching voltage of MoS_2 memtransistor with other representative nonvolatile resistive switching devices, covering printed electronics (MoS_2 RRAM crossbar[9,10] and all WSe_2 1T-1R[12]), hBN (1-R crossbar array,[8] synaptic RRAM,[20] and vdW heterostructure synapse[22]), HfO_xRRAM,[23,24] and standalone MoS_2 memtransistor (back-gate configuration,[13] top-gate configuration,[14] and He-ion beam treated channel.[16]) (f) Conductance map of a 5 × 5 memtransistor subarray. (i) the conductance of 25 memtransistors at HRS. (ii) The memtransistor at the center is set into LRS while the neighboring 24 memtransistors remained at HRS. (iii) The sneak current of the neighboring 24 memtransistors which is represented by the current difference between (i) and (ii).

−60 V and a selected word line (top-gate) voltage of 10 V, which causes significant power consumption. Moreover, previous works based on high-*k* gate dielectric[14] and postgrowth defect engineering using helium-ion irradiation[16] have been employed to reduce the switching voltage, but the switching energy is still larger than nano-Joule which is far from meeting the low-power consumption requirement of in-memory computing.

Here, we demonstrate a 10 × 10 self-selective crossbar array composed of three-terminal memtransistor unit cells with a dense cell size of 3−4.5 F^2 on a continuous monolayer poly-MoS_2 thin film. An optimization of terrace-assisted growth *via* annealing promotes epitaxial MoS_2 growth with orientated

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grains, which effectively enables a low switching voltage of 0.42 V and a switching energy of 20 fJ/bit. The gate terminals of each memtransistor in the same row are connected to form the word lines (WLs), which serve as natural selectors to enable multibit data storage, suppress sneak path leakage current and realize linear and symmetric synaptic weight updating. Furthermore, the circuit simulation using a SPICE-compatible and well-calibrated compact device model confirms a good readout margin and power efficiency. Finally, multiply-and-accumulate operation is experimentally demonstrated by the memtransistor crossbar array, and a MNIST handwritten recognition task is simulated which achieves a pattern recognition accuracy of 96.87%.

RESULTS AND DISCUSSION

Three-Terminal Memtransistor Unit Cell. Monolayer poly-MoS_2 layers are prepared on c-plane (0001) sapphire (Al_2O_3) substrates *via* CVD using MoO_3 powders as Mo precursor and S powders as S precursor in a 2-zone CVD reactor (Supporting Information (SI) Figure S1). Growth of good quality, fully covered continuous monolayer MoS_2 layers on large area substrates (up to 2 in. wafer, Figure 1a) has been realized by carefully optimizing the deposition parameters and growth-setups. A key feature of our CVD method is the use of thin Ni (or NiO)-foam as S-vapor trap to suppress MoO_3 powder poisoning by placing it inside of a closed cylindrical tube containing the MoO_3 precursor (see Figure 1a) or putting it on top of crucible boat containing MoO_3 powders as described in MoS_2 growth in Methods section. Prior to the growth, the sapphire substrate is annealed in air at 1100 °C for 1 h to obtain well-defined terraces on its surface (Figure 1b) which promotes the growth of epitaxial MoS_2 grains on c-plane sapphire.[17] The monolayer characteristic of the synthesized poly MoS_2 is confirmed by Raman and photoluminescence (PL) spectra (SI Figure S2).

The as-fabricated memtransistor array on poly-MoS_2 film is characterized by transmission electron microscopy (TEM), and the cross-section image of a memtransistor is shown in Figure 1c. A gate dielectric made of Al_2O_3 with a thickness of 20 nm is employed while the interlayer dielectric comprises of a 50 nm Al_2O_3 which serves as the insulating oxide for source lines (SLs) formation. The zoom-in image in Figure 1d and SI Figure S3 show a uniform MoS_2 channel thickness down to a monolayer of 0.7 nm, which exemplifies the ultimate scalability. The EDX map of the cross-section and the channel further confirms the uniform distribution of the elements (Figure 1e).

Figure 1f shows the characterization of RS behavior of a single memtransistor cell with 150 consecutive $I_{ds}-V_{ds}$ sweeps at a grounded gate voltage, which exhibits evident bipolar nonvolatile switching. The cumulative probability plot of the high resistance state (HRS) and low resistance state (LRS) at a reading voltage of 0.2 V shows a low temporal (cycle-to-cycle) variation (SI Figure S4). With a defined set current of 10^{-8} or 10^{-7}A, the memtransistor shows a low average switching voltage of 0.42 and 0.62 V (SI Figure S5), respectively, which is 2 orders of magnitude smaller than previous works[13−16] that is critical to realize energy-efficient in-memory computing. The HRS/LRS ratio as read at 0.2 V remains intact through 800 min cycling measurements, implying a long-term nonvolatility (Figure 1g). During the cycling measurements, 80 cycles are performed with an interval of 10 min per cycle, as shown in the top *X*-axis. In contrast to two-terminal RRAM, the memtransistor offers an extra flexibility in deploying both drain and gate terminals to effectively tune the conductance (synaptic weight). The charge accumulation under large V_{ds} and positive gate voltage causes an increase in channel conductance. As shown in Figure 1h and SI Table S1, the current measured with different V_{ds} range and V_{gs} range exhibit eight discrete data storage levels within a large dynamic range of 10^4, which is critical to the computing precision in ANN.

Self-Selective Memtransisor Crossbar Array Operation. The self-selective MoS_2 memtransistor crossbar array architecture and its operating mechanism are schematically described in Figure 2a. Details of the device fabrication steps are described in the Methods section and in SI Figure S6. The drain/gate terminals of memtransistors in the same row are connected to form the bit lines (BLs)/word lines (WLs). The source lines (SLs) connect the source terminals of the memtransistors in the same column together, which run vertically to the BLs/WLs in a separated layer. There is one access transistor connecting each BL/WL/SL in the peripheral circuits outside the array. When setting the memtransistor cells in the crossbar array, as shown in Figure 2a, the selected BL is applied with a voltage V_{set} and the selected WL is grounded or positive biased since the memtransistor shows a *n-type* behavior. The access transistor on the selected source line (SL) is turned on to collect the current. The unselected SLs are switched off by the access transistor and the unselected WLs are floated or applied with negative voltages such that there are no currents flowing through those unselected memtransistors. Figure 2b shows a zoom-in schematic of two neighboring cells which share the same drain to reduce the number of BL to (M/2 + 1) in an M row × N column crossbar array. The crossbar array architecture allows the memtransistors to be independently accessed with a linear *I*−*V* relation under the gate control, so each memtransistor's conductance can be precisely tuned in an analogue manner. Further discussion on the architecture is described in SI Figure S7. To exclude the possible RS caused by metal/Al_2O_3/metal due to the overlap area between SLs and WLs, the *I*−*V* curve is measured in SI Figure S8 which only shows a low current of less than 10^{-11} A without any RS.

The microscopic top-view image of the as-fabricated 10 × 10 MoS_2 memtransistor crossbar array is shown in Figure 2c. The RS curves of the 100 memtransistors are shown in SI Figure S9. It is shown that memtransistors located at the edge show some fluctuations which may compromise the learning accuracy of neuromorphic systems. One mitigation strategy is to use it as a dummy column that remains in minimum conductance state.[18] In the peripheral circuit, the weighted sum of dummy column is subtracted from all the partial weighted sums. This method is especially useful for memtransistors with a limited on/off ratio.[18] A histogram from the inner 64 memtransistors in Figure 2d shows an average set voltage of 0.35 V, which conforms to a normal distribution with a standard deviation σ of 0.04 V when the set current is set at 10^{-8}A, indicating a good spatial homogeneity across devices. An HRS/LRS statistical study of the memtransistors is shown in SI Figure S9. Taking into consideration the current fluctuation of edge devices, as shown in SI Figure S9, a yield of at least 64% is achieved. The uniformity of grain boundaries is a critical factor in controlling device variability, which is not as uniform as the metal/insulator/metal structure such as hBN RRAM in which a high yield of 98% is demonstrated.[19] To achieve a tight control of

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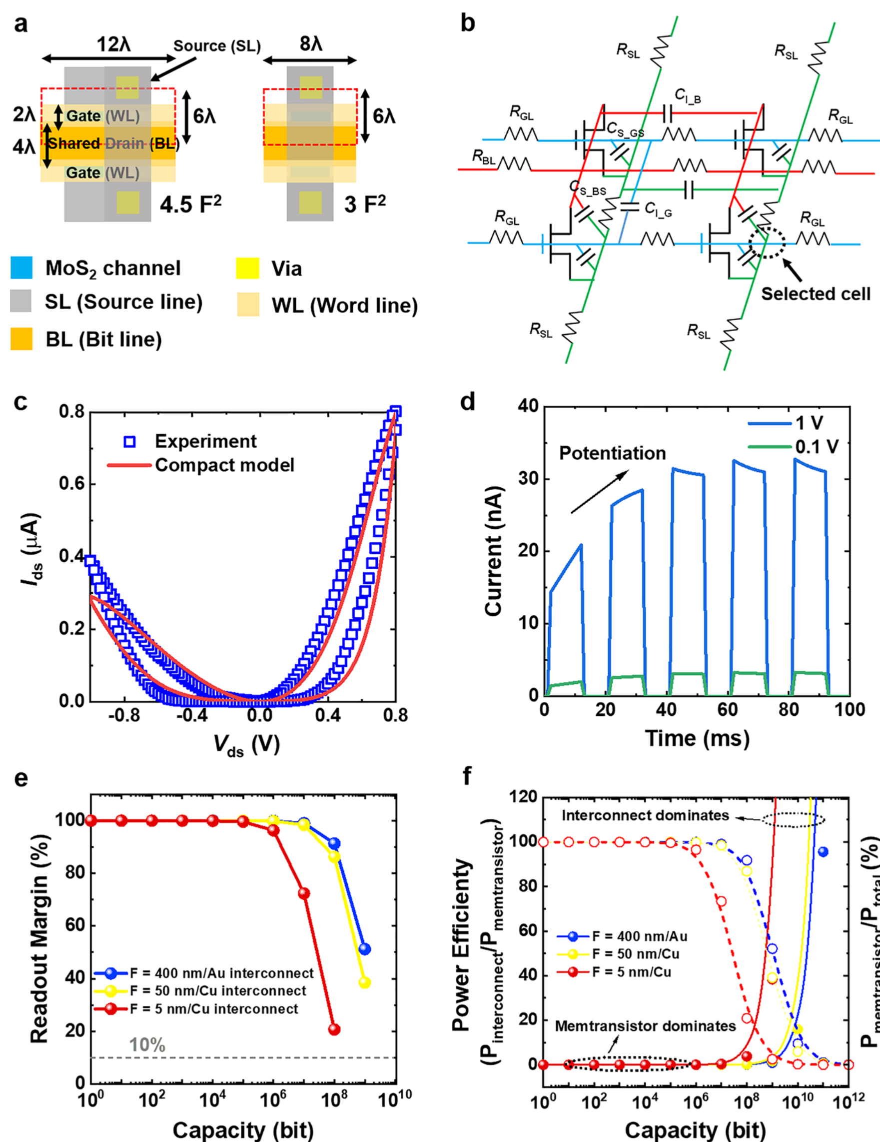

Figure 3. Compact modeling and circuit simulations. (a) Layout of the shared BL structure used in this work with a cell size of 4.5 F^2 and a more compact structure with the source line overlapped with channel, which achieves a cell size of 3 F^2. (b) Circuit diagram of the memtransistor array with parasitic resistance and capacitance. (c) Simulated $I_{ds}-V_{ds}$ from compact model vs. measured MoS_2 memtransistor. (d) Dynamic response of long-term potentiation behavior based on compact model. (e) Readout margin for three different wire resistances simulated by SPICE model. The unit wire resistance is based on Au (blue) used in this work, 50 nm Cu interconnection (yellow) and 5 nm Cu interconnection (red). (f) Simulated power efficiency with the three interconnection schemes mentioned in (e).

device variability, it is important to ensure that grain sizes are much smaller than the channel area (i.e., product of channel length and width) in order to average out the effect of individual grain boundary geometries. Overall, as shown in Figure 2e, our devices show one of the lowest set voltage and switching energy (20 fJ/bit, SI Figure S10) as benchmarked with previously reported MoS_2 memtransistors,[13,14,16] 2DMs (hBN, WSe_2, $MoTe_2$, et al.)[8,9,12,20−22] and transition metal oxide-based memristors.[23,24] Recently, bioinspired protein nanowires memristor has been shown to achieve an even lower switching voltage of 40−100 mV.[25] Moreover, the hBN-based memristor is predicted to achieve a switching energy down to zeptojoule regime if the electrical noise of the semiconductor parameter analyzer could be improved further.[19]

We postulate that the low switching energy is promoted by the oriented grains in the poly-MoS_2 channel.[26,27] It has been well-established that the GBs-facilitated S vacancy movement along the channel, which gives rise to defect profile redistribution, should account for the resistance switching behavior in MoS_2 memetransistor.[14,26,27] Oriented grains bridging the source and drain, and parallel to the direction of current will make the movement of S vacancy more favorable to be triggered, since lower barrier along the channel will be experienced.[27] The sneak current is further studied by programming a pattern in a 5 × 5 subarray and the current difference of unselected devices before and after programming is compared (Figure 2f). First, the conductance of each memtransistor at HRS in a subarray is recorded, as shown in Figure 2f (i). Then the memtransistor at the center is set into LRS wherein the device is subjected to a set voltage of +1 V. The conductance of the selected memtransistor at LRS shows a 30-fold larger as compared with HRS (Figure 2f (ii)). Figure 2f (iii) demonstrates the conductance difference of all the

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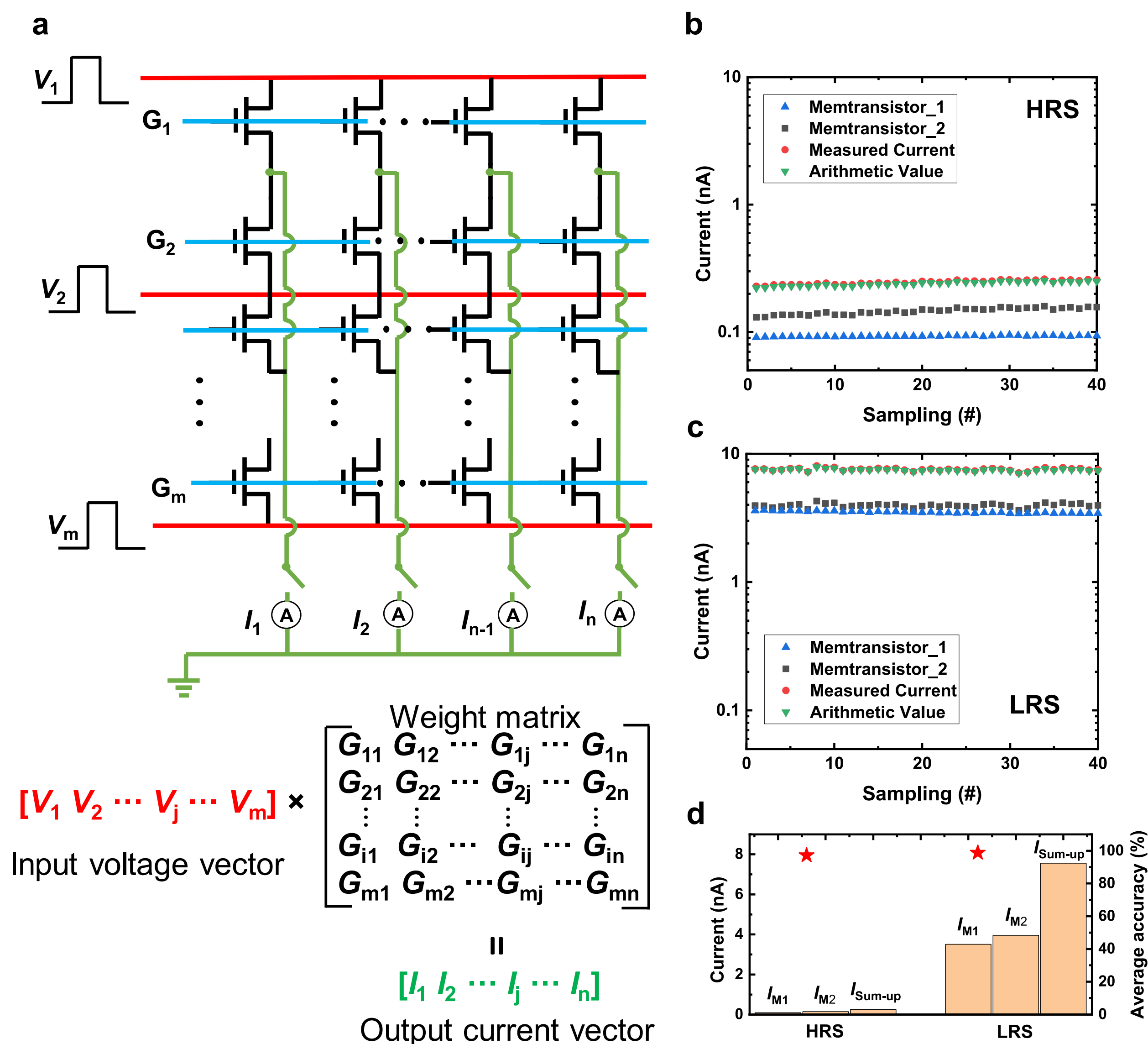

Figure 4. The implementation of multiply-and-accumulate operation by MoS_2memtransistor crossbar array. (a) Circuit diagram of the MoS_2 memtransistor crossbar array and the vector-matrix multiplication principle. Measured and arithmetic currents at (b) HRS and (c) LRS of the two selected memtransistor cells with respect to time. Reading condition: V_{D1} = 0.1 V, V_{D2} = 0.1 V, V_{G1} = 0 V, V_{G2} = 0 V. (d) The currents of two selected memtransistor cells at HRS and LRS, respectively, and the calculated average accuracy.

neighboring unselected devices. It can be seen that the influence to the devices at the nearest two columns is greater than the devices located farther from the selected device. However, it is worth noting that the sneak current remains at a low level of less than 0.1 nA.

Material-Device-Circuit Co-design of Memtransistor Array. With the insatiable technology scaling for increasing memory integration capacity, the voltage drop along the interconnection gradually reduces the voltage available to drive the memtransistor. In order to evaluate the circuit performance, we investigate the material-device-circuit codesign with respect to memtransistor device behavior, physical layout, parasitic effect, and interconnect properties (readout margin and power efficiency) when the integration capacity is increased.

We first analyze the physical layout using λ-based design rule with feature size $F = 4\lambda$ = the minimum half-pitch.[12,28] All the critical feature sizes in the layout are the minimum values which are listed in the Methods section. The left schematic shown in Figure 3a presents a shared-drain layout adopted in this work, which has a cell size of 4.5 F^2. Such cell size is comparable to the 1-R structure (4 F^2), but smaller than the all tungsten diselenide (WSe_2) 1T-1R structure (7 F^2)[12] and the SRAM structure (120−150 F^2).[29] To further reduce the cell size, an even compact structure is shown on the right schematic in Figure 3a wherein the SLs could be fabricated directly on top of isolation oxide. This compact architecture could further reduce the cell size to 3 F^2. By cointegrating the transistor and memristor into a compact memtransistor cell would enable dense on-chip monolithic integration with CMOS logic. The crossbar array is further built by assembling cells into an interconnected network. Figure 3b shows the proposed cell model which includes the wire resistance of BLs/WLs/SLs, the coupling capacitance between two neighboring wires and the stray capacitance between the interconnect wires and the reference plan (source line).[30] The calculation of resistance and capacitance are described in Methods section. To describe the RS behavior, a surface potential-based physical

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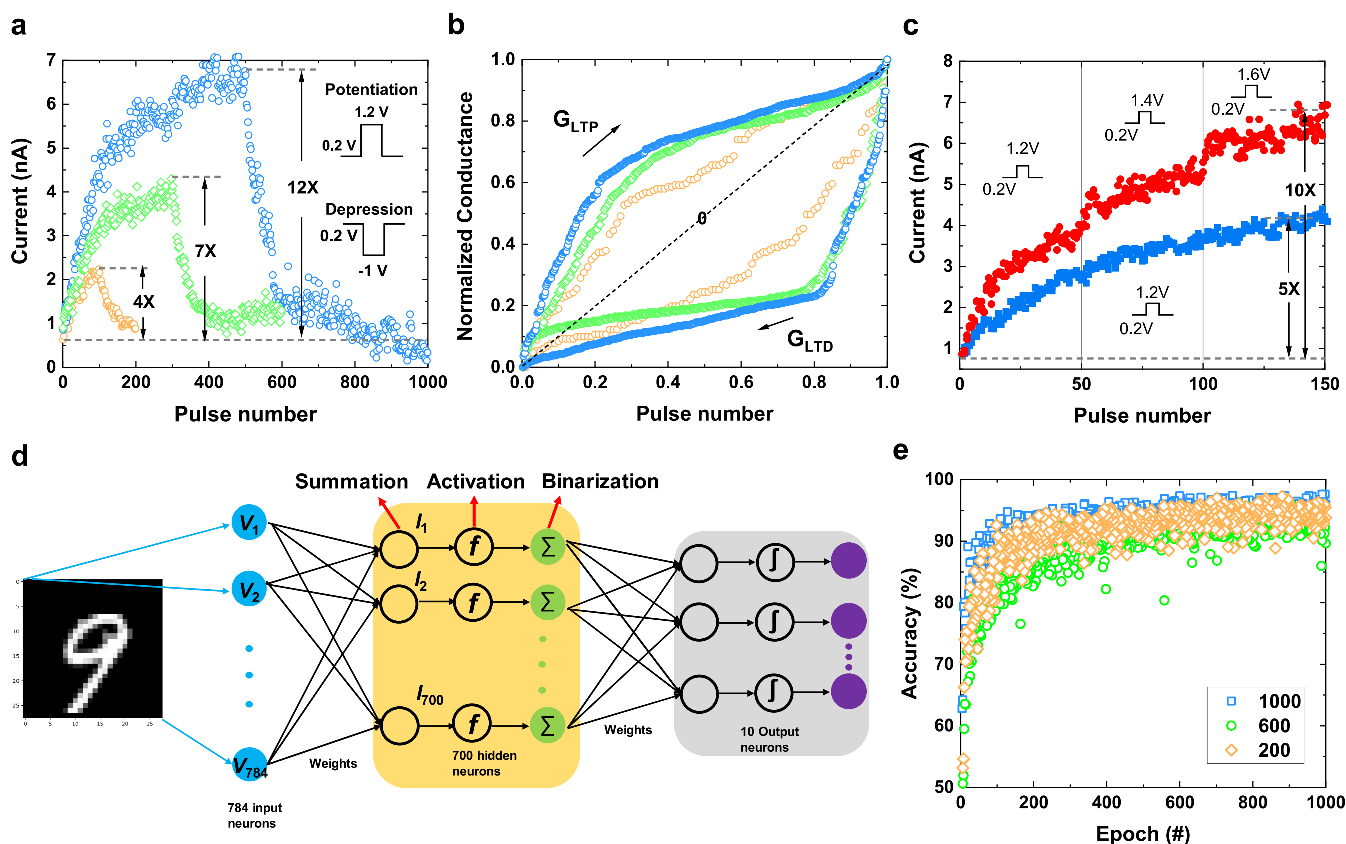

Figure 5. The dynamic response and pattern classification. (a) Potentiation and depression of memtransistor cell with positive/negative pulse train showing the long-term potentiation and long-term depression. The pulse train consists of consecutive set pulses (1.2 V amplitude) followed by consecutive reset pulses (−1 V amplitude). The pulse trains include 100/300/500 positive pulses and 100/300/500 negative pulses, respectively. The current is recorded at a 0.2 V read pulse after each set/reset pulse. Pulse width: 10 ms; Pulse period: 50 ms; $\tau_{up} = \tau_{down}$ = 100 μs. (b) Nonlinearity of the LTP and LTD of three pulse train sets mentioned in (a). (c) The pulse train of 150 set pulses with a pulse amplitude of 1.2 V (blue line) and a pulse train of increased pulse amplitude of 1.2 V, 1.4 V, and 1.6 V, each with 50 set pulses (red line). The condition is the same as that used in (a). (d) A three-layer neural network scheme is employed. (e) Accuracy evolution as a function of training epochs for memtransistor crossbar array with three pulse train sets as shown in (a).

compact model for the memtransistor is utilized.[26,31] The RS behavior is described by the correlation between the dynamics of the total defect/trap density and the grain boundary energy barrier (E_b).[26,31] It is developed on the basis of traditional transport theory in poly material which incorporates grain size dependence. A detailed description of our compact model is described in SI Note S1. The transient and dynamic compact model behavior has been calibrated against the experimental results to validate the model, as shown in Figure 3c and 3d.

The performance of the memtransistor crossbar array is then evaluated by HSPICE with an increase in the integration capacity. In the following discussion, we focus on the worst-case scenario wherein the selected cell is located at the corner furthest from the BL voltage source and the ground, as shown in Figure 3b, where the voltage drop caused by the BL resistance is the largest.[32,33] The readout margin and power efficient are simulated under three process feature size: (1) F = 400 nm for gold interconnect used in this work, (2) F = 50 nm for Cu interconnect used by industry today, and (3) F = 5 nm as projected by ITRS.[30] The readout margin is defined as the voltage imposed to the selected cell under the worst-case scenario over the input voltage, as shown in Figure 3e, which evaluate the voltage drop over the interconnect. It is shown that almost 100% voltage is delivered up to megabit-scale (10^6) capacity for all three different types of wire. The vector matrix multiplication (VMM) operation would be accurate when the interconnect resistance is negligible compared with the memtransistor resistances. The 10% readout margin criterion can support a gigabit-scale (10^9) memtransistor crossbar array using today's Cu interconnect technology with a 50 nm feature size. Figure 3f demonstrates the power efficiency of the interconnection over memtransistor and the memtransistor over the whole circuit. It is shown that as the integration capacity increases, the power consumption induced by interconnect would become a dominant limiting factor. Overall, the results indicate that the need for having a low interconnection resistance is becoming increasingly nontrivial. These results imply the benefits of employing memtransistor crossbar array in simplifying the fabrication process and potentially enabling compatibility with high-volume CMOS manufacturing.

The Implementation of Multiply-and-Accumulate Operation. Mathematically, the in-memory computing can be decomposed into a series of multiply-and-accumulate operations that can be implemented using the memtransistor crossbar array architecture. The equivalent circuit diagram and the vector dot product process is shown in Figure 4a and SI Figure S11. In our methodology, the input signal (encoded as the applied voltage to the BLs) is multiplied with the corresponding weight element (encoded as conductance states

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of the memtransistor), and by utilizing Ohm's law for multiplication and Kirchhoff's laws for accumulation, the weighted sum can be obtained by reading the current in the SL. As can be seen, a voltage vector V_i is applied to the ith row (BLs) while the voltage-induced currents of each memtransistor are collected at the jth grounded columns (SLs). Herein, a total current vector of $I_j = \sum_i V_i G_{ij}$, is collected. During conductance states setting of the selected cells, the selected WLs are grounded or positive biased while all of the unselected WLs are floated or negatively biased to completely deplete the carriers in the channel to avoid sneak current. At the same time, the selected SLs are turned on to collect the current while the remaining unselected SLs are turned off by the access transistors to further avoid sneak current flowing through those unselected memtransistor cells. Moreover, each dot product between the input vector and column vector is noninterfering and thus enables semiparallel programming (column-by-column), which would increase the training efficiency.

Here, we use a subcircuit which consists of two input and one output neurons to perform a basic current accumulation operation, as shown in Figure 4b,c. Figure 4b shows the HRS current of two independent cells in the same column and the current that passes through the corresponding SL. In the off state, the current of both memtransistors show a low level of 0.1 nA, which indicates an excellent isolation between the selected and unselected cells with minimal sneak current flowing through. Then the two memtransistors are set into LRS simultaneously with a set voltage of 1 V. After setting into LRS, as shown in Figure 4c, the programmed states over the initial states show a 10-fold difference for both memtransistor cells. For both the HRS and LRS, the multiplication products equal to the summed current through the SLs, as shown in Figure 4d. As compared with the arithmetic results, the measured results demonstrate an accuracy of 97.17% and 98.76%, respectively. Overall, the experimental demonstration indicates a good control over gate leakage current and sneak current, which implies its potential to perform VMM using larger scale crossbar arrays.

Synaptic Plasticity and Pattern Classification Simulation. To implement VMM-based neural network algorithm, we first characterize the long-term plasticity which is used to store trained synaptic weights for each layer in the artificial neural network (ANN). Figure 5a shows the long-term potentiation/depression for three different positive/negative stimulus with a pulse width of 1 ms and a pulse amplitude of 1.2 V. The conductance update shows a gradual and linear increase/decrease manner as compared with filamentary RRAMs which usually experience a sudden drop due to the stochastic dissolution of conductive filaments.[34] Thus, RS based on electric-field mediated defect migration is probably a more reliable mechanism for enabling an analogue conductance update. Moreover, the analog on/off ratio is increased to more than 10 when the pulse number is increased from 200 (100 potentiation/100 depression) to 1000 (500 potentiation/500 depression). The nonlinearity and symmetry of LTP and LTD are further quantified using a device behavioral model,[35] as shown in Figure 5b. With 200 LTP/LTD pulses, the plasticity behavior becomes closer to an ideal linear and symmetric learning rule that is desirable for ANNs. The increased number of pulses enable more conductance states and a larger dynamic range, however, at the expense of a higher nonlinearity after the conductance reaching its maximal value. A mitigation strategy to avoid the saturation is to apply a pulse train with potentiated voltage amplitude. As shown in Figure 5c, with an increased pulse amplitude from 1.2 to 1.6 V, the dynamic ratio is increased by 10-fold with a stimulation of only 150 pulses, showing a better linearity as compared with a 1.2 V pulse train.

On the basis of the measured characteristics from a standalone memtransistor, pattern classification workload is selected as a case study algorithm wherein an ANN is modeled to perform a supervised learning using the Modified National Institute of Standards and Technology (MNIST) handwritten recognition data set. As schematically shown in Figure 5d, a fully connected multilayer perceptron (MLP) ANN with 28 by 28 preneurons, 700 hidden neurons and 10 output neurons is generated by software. The 784 neurons of the input layer correspond to a 28 × 28-pixel black-and-white MNIST image, and the 10 output neurons correspond to 10 classes of digits (0−9). The weighted sum of the input vector and the synapse matrix is processed through a sigmoid activation and a binarization function and then propagated to the output layer. The gradient descent optimization algorithm is adopted to adjust and update the weights, wherein the amount of delta weight is calculated and back-propagated to the synapse matrix. The optimization is iterated until the minimized loss function that measures the error between the output and target values is obtained. For the simulation, we consider two nonideal factors of the memtransistor, that is, the finite number of conductance levels and the device-to-device variation. First, the weights are represented by the measured finite conductance levels in Figure 5a. Since the weights used in algorithm can be either positive or negative values ($W_A = -1-1$), while the measured weights in Figure 5a can only represent positive values ($W_H = 0-1$), here a reconstruction $W_A = 2\ W_H - 1$, is performed to expand W_H to the range of W_A.[18] Second, the device-to-device variation (SI Figure S9c) is analyzed by introducing the variation to the weight initialization step. The training set comprises of 60 000 images which are randomly selected from the MNIST data set and a separate testing set of 10 000 images. The simulation results in Figure 5e show that MoS_2 memtransistor ANN can achieve a recognition accuracy of up to 96.87%, which is comparable to the accuracy of other memristors-based ANN.[18,36]

CONCLUSION

In this work, a memtransistor crossbar array architecture capable of performing multiply-and-accumulate operation is implemented to solve data-centric tasks in pattern recognition, which could be extended to other AI-driven applications such as speech recognition, autonomous vehicles, among others. The use of three-terminal architecture with electrostatic gate effect provides an additional knob to effectively suppress sneak current, enables a linear and symmetry synaptic plasticity, and a practical readout margin for gigabit-scale integration. The ability to individually control each memtransistor also enables semiparallel programming (column-by-column) of the entire array, resulting in high training efficiency. Notably, the added functionality is realized with our memtransistor crossbar array architecture without any circuit footprint penalty, which is superior over other traditional three-terminal unit cells (e.g., 1T-1R, flash memory or FeFET). The promising results demonstrated by the MoS_2 memtransistor crossbar array hold tantalizing prospect to realize practical neuro-inspired computing chips for deep neural networks and edge computing in the coming age of AI and IoT.

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METHODS

Fabrication Process of Memtransistor Crossbar Array. Monolayer polycrystalline MoS_2 growth is performed in a 2 zone CVD furnace with 1.5 g sulfur (99.998%, Sigma-Aldrich) positioned in the upstream zone at 150 °C and 3.5 mg MoO_3 (99.98%, Sigma-Aldrich) positioned in the downstream zone at 750 °C with an Ar gas flow of 50 sccm. The growth process is done with the tube maintained at a pressure of 6 Torr. Both temperatures are held for 10 min before being allowed to cool naturally to 600 °C before the furnace hatches are open for rapid cooling. MoO_3 and S powders are placed 30 cm apart. MoO_3 powder is placed in a single open-end crucible with a piece of nickel foam (size 3 cm × 3 cm, 1 mm thickness with 400 μm average pore size) placed directly above the MoO_3 powder. The sapphire substrate is placed above the foam, supported by pieces of ceramic. The substrate used is a commercially bought c-plane (0001) sapphire (Al_2O_3) substrate (Namiki Inc.) that has been annealed in air at 1100 °C for 1 h before being used for CVD growth of MoS_2. This growth method is adapted from a previously reported work.[37]

The memtransistor crossbar array is directly fabricated on the as-used sapphire substrate. A 10 × 10 array of MoS_2 active regions are first defined by a laser writer (LW405B) and then etched using CHF_3/O_2 reactive-ion etching (RIE, Oxford Plasma Pro100) process. The etching recipe could be found in our previous work.[38] Then MoS_2 memtransistor channel (length: 400 nm, width: 20 μm), the bit lines (BLs) which connect the drain terminal of the memtransistors in the same row and the BL contact pad are defined by an electron beam lithography (EBL: Jeol-6300FS) wherein PMMA (495, A4) is spin-coated with a rotation speed of 4000 rpm for 70 s. This is followed by 10 nm Ti/40 nm Au evaporation by an AJA electron beam evaporator and lift-off. After that, 20 nm Al_2O_3 gate dielectric is deposited by atomic layer deposition (Savannah ALD) at 150 °C using trimethylaluminum (TMA) and H_2O precursors. Then the word lines (WLs) which connect the gate terminal of the memtransistors in the same row are formed. The WLs and the contact pads are written using a laser writer and then the 10 nm Ti/40 nm Au metals are deposited by e-beam evaporator. After lift-off process, 50 nm Al_2O_3 is deposited to form the isolation oxide using the same gate dielectric deposition recipe. Then laser writer is used to expose the Via patterns wherein AZ1512 is used as the photoresist and the soft mask for the following Via etch process. The AZ1512 is spin-coated with 6000 rpm for 70 s. The dilute KOH solution is subsequently used to etch the Vias wherein the 50 nm Al_2O_3 oxide and 20 nm Al_2O_3 beneath the Via patterns are totally etched away in around 1 h. Finally, a third laser writer process is performed to write the source lines and the corresponding metal pads. Finally, 10 nm Ti/40 nm Au is evaporated and lifted-off to fill the Vias and formed the SLs.

The morphology of poly-MoS_2, especially the grain boundary, is characterized using a Bruker Dimension FastScan Atomic Force Microscope (AFM) in the tapping mode. The channel width and length are determined by a Scanning Electron Microscopy (SEM, FEI Helios). The cross-section of the memtransistor crossbar array is obtained by high-resolution transmission electron microscopy (HRTEM, FEI Tecnai F20). The focused ion beam (FIB) technique is employed to prepare a lamella, used for obtaining a cross-sectional image from the top metal gate to the sapphire substrate.

Electrical Measurement Techniques. Electrical measurements are carried out in air condition at room temperature with a semiconductor parameter analyzer (Keithley 4200) equipped with pulse measurement units and a Lakeshore probe station.

SPICE Simulation of the Memtransistor Array. The RS curve and the LTP of the memtransistor cell in Figure 3c,d are modeled using Verilog-A. The readout margin and power consumption of large-scale crossbar array is simulated using HSPICE.

All the critical feature sizes in the layout are the minimum values according to the MOSIS deep submicron lambda rule: metal width 4F; metal space 4F; gate width 2F; contact width 2F; metal enclosure contact 1F.

The evaluation details of the wire resistance are as below: suppose the feature size is F (400 nm Au, 50 nm Cu, 5 nm Cu), the aspect ratio (L/W) is set to be 1, and wire thickness is set to be H = 40 nm. The resistivity of Au, 50 nm Cu and 5 nm Cu is 2.27 $\mu\Omega$·cm, 4.77 $\mu\Omega$·cm, 14.41 $\mu\Omega$·cm, respectively. The wire resistances of WL/BL/SL are calculated using $R = \rho \cdot L/W \cdot H$. The capacitance is calculated by the parallel plate capacitor model $C = \varepsilon_0\ \varepsilon_r\ (A/d)$ where ε_0 is the value of the permittivity for air which is 8.84×10^{-12} F/m, and ε_r is the permittivity of the dielectric material Al_2O_3 which is 9.1.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.0c09441.

Figures S1−S11: Materials and characterization, device design, experimental details, measurement data, and simulation. Table S1: Average current and standard deviation statistics. Note S1: Description of the compact model (PDF)

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Author Contributions

K.-W. A. supervised the project. K.-W. A. and X. F. conceived the idea and designed the experiments. X. F. performed most of the experiments and simulations. S. L.W. and S. T prepared the MoS_2 films. S. L and L. C assisted in the pulse measurement. P.Z, and L.W. assisted in the compact model

development. All authors discussed the results and contributed to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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