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Artificial Synapses Based on Multiterminal Memtransistors for Neuromorphic Application

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Neuromorphic computing, which emulates the biological neural systems could overcome the high-power consumption issue of conventional von-Neumann computing. State-of-the-art artificial synapses made of two-terminal memristors, however, show variability in filament formation and limited capacity due to their inherent single presynaptic input design. Here, a memtransistor-based artificial synapse is realized by integrating a memristor and selector transistor into a multiterminal device using monolayer polycrys-talline-MoS_2 grown by a scalable chemical vapor deposition (CVD) process. Notably, the memtransistor offers both drain- and gate-tunable nonvolatile memory functions, which efficiently emulates the long-term potentiation/depression, spike-amplitude, and spike-timing-dependent plasticity of biological synapses. Moreover, the gate tunability function that is not achievable in two-terminal memristors, enables significant bipolar resistive states switching up to four orders-of-magnitude and high cycling endurance. First-principles calculations reveal a new resistive switching mechanism driven by the diffusion of double sulfur vacancy perpendicular to the MoS_2 grain boundary, leading to a conducting switching path without the need for a filament forming process. The seamless integration of multiterminal memtransistors may offer another degree-of-freedom to tune the synaptic plasticity by a third gate terminal for enabling complex neuromorphic learning.

1. Introduction

Inspired by the human brain, neuromorphic computing on the hardware level is a data processing model that could address the inherent energy and throughput limitations of conventional von-Neumann computing architecture, which holds promise for achieving high efficiency in performing cognitive and data-intensive tasks.[1–5] In neuromorphic computing system, artificial synapse is a class of fundamental functional component (the other is neuron) that enables the transmission of information from one neuron to another with updated synaptic weight (i.e., electrical conductance of the device). To date, applications for artificial synapses have been widely investigated in many memristor-based devices, such as phase change memory (PCM),[6] resistive random access memory (RRAM),[3,7–9] ferroelectric field-effect transistors (FeFET),[10,11] and floating-gate field-effect-transistors (FGFETs).[12–14] In the past years, 2D layered semiconductors have

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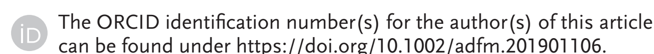
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been under active study for synaptic device application.[7,12,14–21] In a typical configuration, they are used as channel materials to implement transistor-based synapses, which exhibit large hysteresis in the transfer characteristics, thus can be used to mimic the synaptic functionality by applying electrical stimulation to the gate. Concerning gate dielectrics, both conventional oxide insulators and native oxide of 2D materials have been explored.[12,14] Particularly, by using polymer electrolyte laterally coupled gate dielectrics, coplanar-gate 2D-based transistors have been extensively investigated for synapse application, operated with low spike voltage.[19–21] Furthermore, by deploying coplanar-multigate structure, novel functions have been demonstrated such as photoelectronic and spatiotemporal hybrid neuromorphic integration, and spatiotemporal coordinate and orientation recognition.[22,23] Nevertheless, these works have relied on the mechanical exfoliation of layered materials for device fabrication, which hinders their practical application due to lack of scalability. In parallel, Sangwan et al. demonstrated bottom-gate memtransistors made from polycrystalline layered transition metal dichalcogenide material. The memristive switching behavior was attributed to the dynamic modulation of Schottky-barrier height at the source and drain end of the device originating from the grain-boundary-mediated migration of sulfur vacancy defects.[18,24] Compared with traditional metal–insulator–metal (MIM)-structured two-terminal devices, the memtransistors offer another degree of freedom for synaptic weight modulation and further enable emulation of heterosynaptic plasticity. Nevertheless, in previous works, for emulating synaptic functions, the input of electrical excitation was limited to one particular terminal of the device (i.e., gate for synaptic transistors[12] and drain for memtransistors[24]) and the operating voltages were relatively high (40 V voltage pulse).

Here, we report a multiterminal memtransistor-based artificial synapse made of monolayer polycrystalline-MoS_2 for neuromorphic computing. The MoS_2 film was grown via scalable chemical vapor deposition (CVD) approach and the entire device fabrication process is compatible with existing technology, implying its potential towards practical application. The memtransistors exhibit a significant analog-resistive switching behavior with switching ratio exceeding 10^4, which is promising for large-dynamic-range neuromorphic application. By employing high-κ gate dielectric, the devices permit a much lower operation voltage compared with other transistor-like synaptic devices, and can efficiently emulate the key synaptic activities including long-term plasticity, spike-amplitude-dependent plasticity (SADP), and spike-timing-dependent plasticity (STDP). Furthermore, unlike previous artificial synapses that are restricted by single presynaptic input, our devices allow both the gate and drain terminals to serve as the stimulus input, thus offering more flexibility for designing complex neuromorphic circuits, demonstrating its potential for realizing brain-like artificial intelligence systems.

2. Results and Discussion

Continuous polycrystalline MoS_2 film was grown via chemical vapor deposition on a quarter 2-inch sapphire substrate (**Figure 1**a).[25] The monolayer characteristic of the synthesized film was confirmed by Raman and photoluminescence (PL) spectra (Figure S1, Supporting Information). Atomic force microscopy (AFM) reveals grain sizes of 1–3 µm of the MoS_2 film (Figure 1b). Figure 1c shows the schematic of the array top-gated memtransistors, which were directly fabricated on the as-used sapphire substrate in the absence of a transfer process (Figure 1d). Devices were fabricated with various channel lengths ranging from 200 nm to 8 µm. 5/70 nm Ti/Au were deposited by electron beam evaporation for forming source, drain, and gate electrodes. Details of the device fabrication are given in the Experimental Methods (In Supporting Information). The fabricated devices were additionally characterized by cross-sectional transmission electron microscopy (TEM). The TEM image reveals the lattice disorders within the device channel (Figure 1e), in good correspondence to the polycrystalline nature of the MoS_2 film.

We first characterized the fabricated MoS_2 memtransistor by sweeping V_{ds} in a closed loop at V_{gs} = 0 V. **Figure 2** presents the result on a 400 nm channel length memtransistor. In Figure 2a, by sweeping V_{ds} in various ranges from −6 V and 6 V to between −12 V and 12 V, the device shows evident bipolar analog resistive switching (RS) behavior. Specifically, starting from V_{ds} = 0 V, a positive scan of V_{ds} toward higher positive biases gradually switches the device from the high resistance state (HRS) to its low resistance state (LRS) and retains its LRS for V_{ds} sweep back to 0 V. Meanwhile, a reset to HRS can be achieved by sweeping a negative V_{ds} and the HRS is maintained for V_{ds} from −10 to 0 V. It is evident that the HRS and LRS of the device are largely affected by the V_{ds} sweep range, the mechanism of which will be discussed later. The resistances corresponding to the HRS and the LRS are extracted using the currents at V_{ds} = 0.1 V and plotted in Figure 2b. Apparently, the ratio between HRS and LRS enlarges with increased V_{ds} range. Consequently, the calculated switching ratio, defined as R_{HRS}/R_{LRS}, changes from 34 for ±6 V to >10^4 for ± 12 V (Figure 2c), manifesting the wide tunability of resistive states. To investigate the endurance of the gradual RS characteristic, I_{ds}–V_{ds} curves were recorded by continuously sweeping V_{ds} in a closed loop between −10 V and 10 V. As shown in Figure 2d, no significant differences are noticed for the consecutive 160 sweep cycles, indicating good endurance when operating as a memristor. It is worth noting that we have carried out more than 800 measurement cycles on another device that also shows excellent endurance property (Figure S2, Supporting Information). Notably, by extracting the HRS and LRS resistance values of the device (currents at V_{ds} = 0.1 V were used), a switching ratio higher than 10^4 is obtained (Figure 2e,f), outperforming previously reported devices with similar configurations.[12,14,24]

In addition to the dependence of RS on V_{ds} range, the device also exhibits gate-tunability function, rendering it a so-called memtransistor. Figure 2g plots the device switching loops by varying V_{gs} from −6 V to 4 V in a step of 2 V for V_{ds} sweep range between −6 V and 6 V. Apparently, both the HRS and LRS manifest a large gate dependence. Compared with the resistance switching at V_{gs} = 0 V, a much wider range of the HRS and LRS can be obtained by gate modulation, consequently giving rise to a tunable switching ratio from 500 to 10 for V_{gs} = −6 V and V_{gs} = 4 V, respectively (Figure 2h,i). Considering the results in Figure 2a, a more remarkable gate dependence can be fully anticipated by applying a wider range of V_{ds}. The momentous

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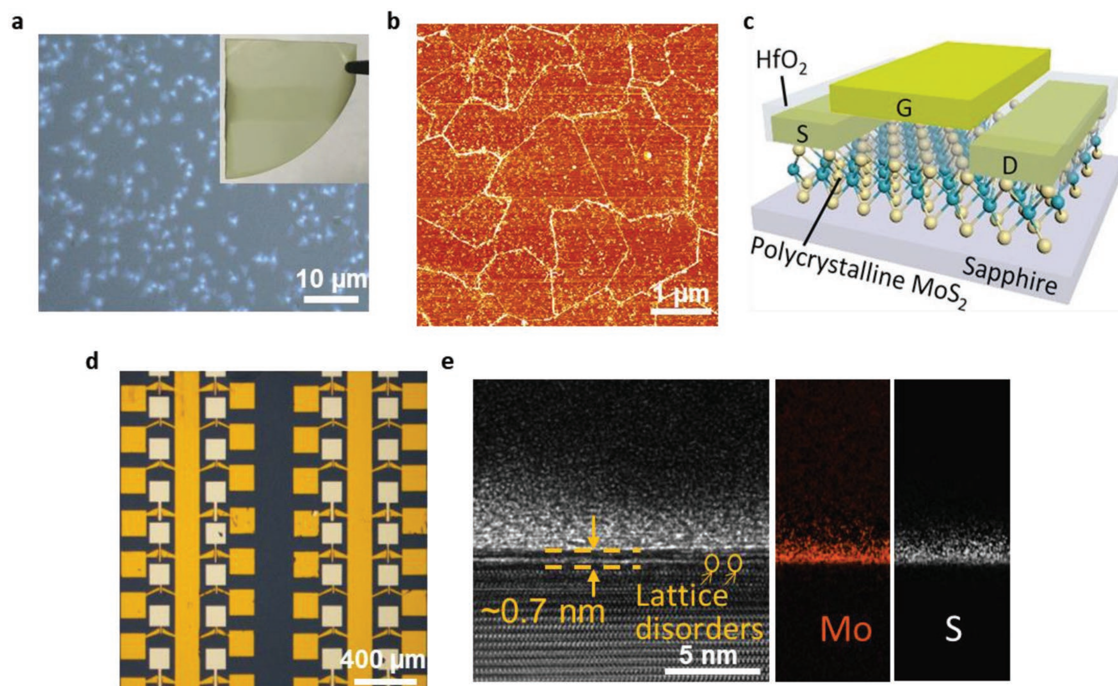

Figure 1. Polycrystalline monolayer MoS_2 characterization and memtransistor fabrication. a) An optical micrograph of the continuous polycrystalline MoS_2 thin film grown on a transparent sapphire substrate via a CVD process. b) Scanned atomic force microscopy (AFM) phase channel image in the tapping mode over an area of 5×5 µm^2, revealing grain sizes of 1–3 µm with distinct grain boundaries within the film. c) A schematic of the fabricated MoS_2 memtransistor in a top-gated field-effect-transistor (FET) configuration on the as-used sapphire substrate. 20 nm HfO_2 was used as the gate dielectric. d) An optical micrograph of the MoS_2 memtransistors after fabrication. Devices with different channel lengths were fabricated. e) TEM image of the cross-section of a monolayer MoS_2 transistor along the device channel. Defects of lattice disorders are revealed, corresponding to grain boundaries in the MoS_2 film. On the right shows the EDX mapping of the element of Mo and S, confirming MoS_2 as the channel material.

dependence of the device's analog switching characteristic on V_{ds} and V_{gs} implies great flexibility for emulating complex synaptic connections. Compared with traditional two-terminal memristors, the integration of memristor within a transistor structure offers another degree of freedom to achieve a wider tunability of multiple-level states by gate modulation.[26]

The gradual RS behavior in V_{ds} closed-loop sweep can be attributed to the grain-boundary-mediated defects migration under high electric field in the channel. Here, we performed first-principles calculations to understand the defect migration energetics and mechanisms. We noticed that for longer channel (>1.5 µm) memtransistors, they give rise to a significantly weaker drain current in the positive-V_{ds} regime accompanied by a moderate switching ratio (Figure S3, Supporting Information). The difficulty in them being switched on is likely related to the less-efficient defects migration as a result of weaker electric field in the channel. Furthermore, the RS behavior is found to be absent in the floating gate case (Figure S4, Supporting Information), which implies the importance of gate effect in the RS process. In general, the RS behavior should primarily originate from the defects in MoS_2. Various defects in MoS_2 have been observed experimentally,[27–30] such as single vacancy S (V_S), double vacancy S (V_{2S}), (5|7) Mo–Mo dislocation, and (4|6) defect complex comprising a (5|7) S–S dislocation and a double S vacancy V_{2S}. Our calculations show that the diffusion barriers of V_S and V_{2S} are 2.297 and 4.149 eV in perfect monolayer MoS_2 (Figure S5, Supporting Information). These energy barriers are simply too high to give rise to the RS observed experimentally. We further study the diffusion barriers of these two vacancies along a stable (5|7) Mo–Mo grain boundary in polycrystalline MoS_2. Previous work has shown that the (5|7) defect in an S-polar GB energetically favorably converts to the (4|6) defect forming one V_{2S}, and the (5|7) Mo-polar GB are stable.[30] Here, we focus on the migration of the (4|6) defect complex. The possible diffusion path and diffusion barrier for V_{2S} in the polycrystalline MoS_2 are shown in Figure S5 (Supporting Information). Based on our computed energy barrier, the V_{2S} is shown immobile along the GB direction. We further investigate V_{2S} migration perpendicular to the GB direction, and the initial (IS) and final (FS) states are shown in **Figure 3**a. The calculated energy barrier for V_{2S} diffusion with the aid of (4|6) dislocation sliding is merely 0.656 eV (Figure 3b), which is much lower than the energy barrier of V_{2S} diffusion parallel to the GB direction (4.865 eV). Based on the calculated energy barriers of V_{2S} migrated along the perpendicular direction, we conclude that V_{2S} may diffuse easily with the aid of (4|6) dislocation moving perpendicular to the GB direction, and the RS effect observed in polycrystalline MoS_2 may originate from this diffusion mechanism.

Moreover, an external electric field applied across polycrystalline MoS_2 will provide a driving force for the drifting of charged (4|6) defect complexes. At the nanoscale, a small voltage may yield a large electric field, which provides a large driving force for charge transport. We break the periodic boundary condition along the V_{2S} hopping direction (*z*-direction in our computational model) by applying an external electric field

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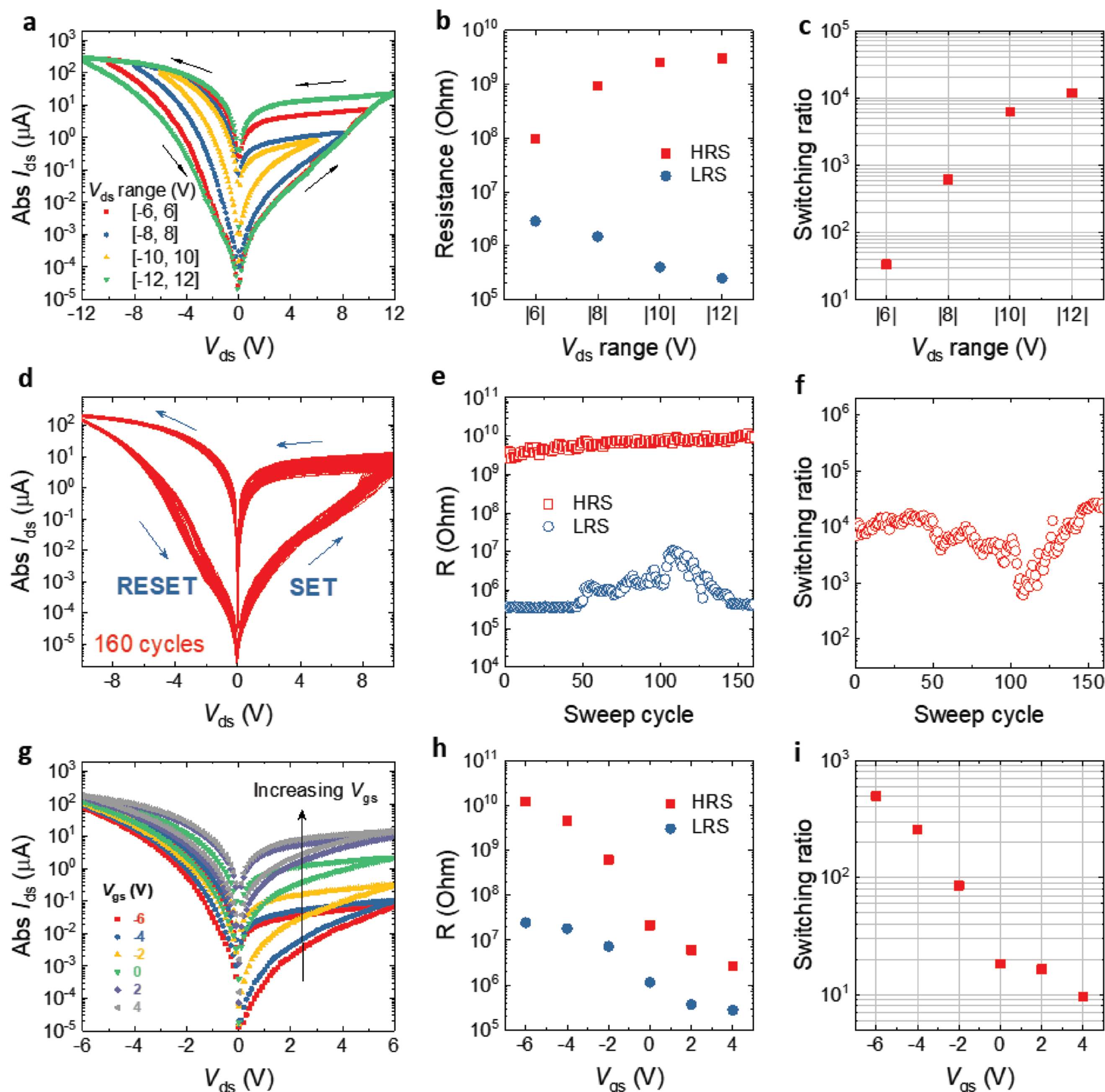

Figure 2. Electrical characterization of a representative MoS_2 memtransistor with a channel length L = 400 nm and a channel width W = 30 µm. a) Looped current–voltage characteristics (I_{ds}–V_{ds}) of the device at various V_{ds} sweep range of from −12 to 12 V, from −10 V to 10 V, −8 V to 8 V and −6 V to 6 V at V_{gs} = 0 V, showing evident bidirectional gradual resistive switching (RS) behavior. Direction of the sweep is indicated by the black arrows. b) Resistance values corresponding to the high-resistance-state (HRS) and the low-resistance-state (LRS) of the device for different V_{ds} sweep ranges. Currents at V_{ds} = 0.1 V were used for calculation. c) Calculated switching ratio (R_{HRS}/R_{LRS}) as a function of V_{ds} sweep range, showing an increasing trend with the increase of V_{ds} sweep range. d) Endurance of the RS behavior of the MoS_2 memristor by recording I_{ds}–V_{ds} characteristics for 160 consecutive cycles for V_{ds} between −10 and 10 V at V_{gs} = 0 V. The blue/green arrows indicate V_{ds} sweep direction. e) Resistances corresponding to the HRS and the LRS during the 160 sweep cycles, revealing a good endurance property of the device. Currents at V_{ds} = 0.1 V were used for calculation. f) Calculated switching ratio as a function of cycle number. Switching ratios of higher than 10^4 are obtained. g) MoS_2 memtransistor exhibiting gate-tunability of the memristive behavior. V_{ds} is swept in the range between −6 and 6 V in a closed loop at varying gate potentials from −6 to 4 V in a 2 V step. h) Extracted HRS and LRS resistances at V_{ds} = 0.1 V. i) Calculated switching ratio as a function of V_{gs} showing a gate-bias dependence. A scan rate of 2 V s^{-1} was used.

varying between −0.5 to 0.5 eV Å^{-1} perpendicular to the (4|6) dislocation GB as shown in the inset of Figure 3c. The positive field direction is defined as the same direction as the V_{2S} with (4|6) dislocation movement. Our calculation results reveal that the diffusion barrier has a nearly linear relation with the applied external electric field. The predicted diffusion barrier

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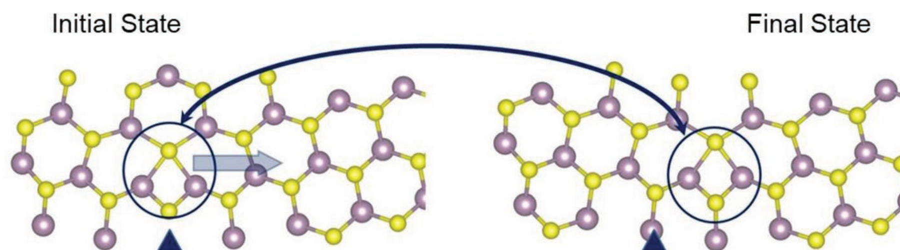

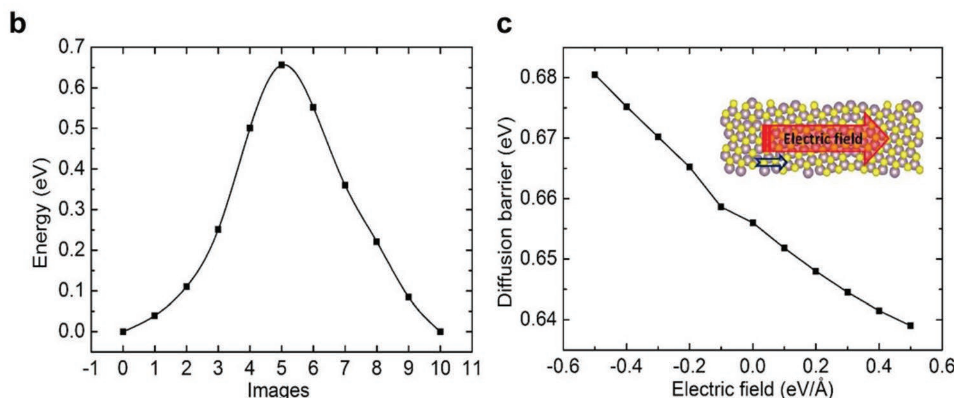

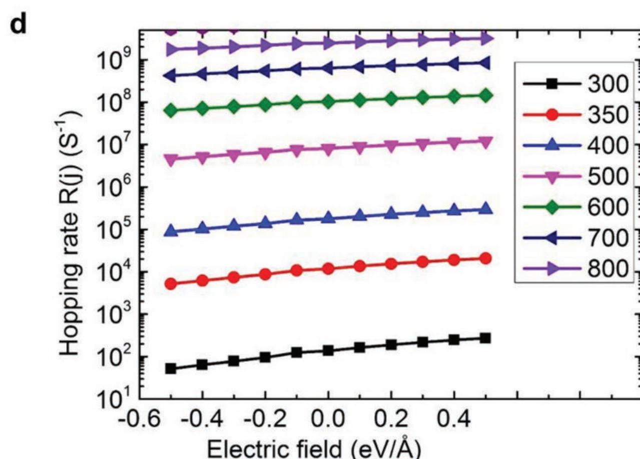

Figure 3. First principles calculation results for S vacancy diffusion in the polycrystalline MoS_2. a) The initial and final states of V_{2S} perpendicular to the GB. The inserted blue triangles are the reference showing the (4|6) dislocation movement. The blue and yellow balls represent Mo and S atoms, respectively. b) The diffusion barrier of V_{2S} diffusion perpendicular to the (4|6) GB. c) The electric field-dependent diffusion barrier of V_{2S} diffusion perpendicular to the (4|6) GB. d) The temperature effect to the electric field-dependent diffusion barrier of V_{2S} diffusion perpendicular to the (4|6) GB.

is 0.681 eV when the electric field is –0.5 eV Å^{-1}, decreases to 0.656 eV when there is no external electrical field, and further decreases to 0.639 eV when the electric field is 0.5 eV Å^{-1}. A similar trend was also observed for Pt atom on Pt (001) surface under an applied electric field.[31] According to our calculated electric field-dependent diffusion barrier, we further predict the hopping rate of V_{2S} under an external electric field at temperature T based on the equation of $R_j = \nu_0 \exp(-G_b/k_B T)$, where ν_0 is an attempted frequency related to the frequency of atomic vibrations and is usually taken as the Debye frequency. ΔG_b is the calculated diffusion energy barrier, and k_B is the Boltzmann constant. We use the reported Debye temperature of 262.3 K to compute the hopping rate R_j of V_{2S} under an external electric field at a temperature between 300 and 800 K,[32] as shown in Figure 3d. It is seen that the effect of electric field on the diffusion hoping rate becomes weaker at higher temperature due to thermal effect. At room temperature (300 K), the hopping rate is 2.73×10^2, 1.37×10^2 and 5.18 s^{-1} under the external electric field of 0.5, 0 and –0.5 eV Å^{-1}, respectively. When temperature is increased to 800 K, the hopping rate is 3.18×10^9, 2.48×10^9, and 1.74×10^9 s^{-1} under an external electric field of 0.5, 0, and –0.5 eV Å^{-1}, respectively. According to our calculation results, at room temperature (i.e., 300 K), the hopping rate of V_{2S} under 0.5 eV Å^{-1} is two times that under

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0 eV Å^{-1}, and about two orders that under −0.5 eV Å^{-1}. Hence, the DFT results can well explain the experimental observations as shown in Figure 2. Without the electric field effect, V_{2S} has a fixed diffusion barrier, and the device should exhibit consistent RS. Due to the ability of the electric field in modifying the V_{2S} diffusion barrier and hopping rate, the device displays an evident bipolar analog RS behavior through sweeping the V_{ds} range from between −6 and 6 V to between −12 and 12 V.

Next, the devices are examined to emulate the synaptic plasticity of biological synapses. Sequential voltage pulses are introduced to the drain terminal as presynaptic input while the drain-source current is continuously recorded as postsynaptic current (PSC, I_{ds}) (**Figure 4**a). The long-term potentiation (LTP) and long-term depression (LTD) behaviors of the artificial synapse are demonstrated in Figure 4b. It is shown that a positive V_{ds} pulse sequence of +10 V and a negative V_{ds} pulse sequence of −10 V (1 ms width) induce positive and negative exponential changes in PSC, respectively. Moreover, a shorter pulse duration (100 µs) gives rise to a relatively slow potentiation and depression process, thus requiring more pulse number to achieve the same change in PSC (Figure 4c). The dynamic process of LTP and LTD of the memtransistor under voltage pulses with different amplitudes is shown in Figure 4d,e, respectively. It is seen that a larger pulse amplitude results in a faster potentiation or depression. We note the relatively low current for positive V_{ds} pulses than for negative V_{ds} pulses, which is likely associated to the channel current saturation tendency on positive V_{ds} side as a result of the *n*-type conduction of MoS_2. Figure 4f presents the evolution of PSC under a consecutive pulse sequences with varying pulse amplitude. As is seen, the PSC continues to increase with positive V_{ds} pulses, and as the pulse amplitude augments, the PSC increases more rapidly. This can be more clearly noticed from the change in PSC after 50 pulses of each sequence (Figure 4g), which exhibits an enhancement with increasing V_{ds} pulse amplitude, implying the ability of memtransistor in responding to different-amplitude stimulation, or SADP. In a neuromorphic system, STDP is another important functionality for the learning and memory process. It describes the dependence of synaptic plasticity on the temporal distance between sequential action potentials, and can be mimicked by using paired voltage pulses separated by a time interval. In a typical scenario, longer positive time interval results in a weaker potentiation, and longer negative time interval leads to a slower depression of the synaptic strength. For our device, by making use of paired pulses distanced by a time interval, its ability to mimic indirect STDP is examined.[24] As shown in Figure 4h, positive (negative) changes in the synaptic weight are induced by positive (negative) V_{ds} pulses, with longer time interval leading to weaker potentiation (depression). By fitting the data using an exponential model, the time constants for potentiation and depression responses are derived[33,34] to be 11.6 and 6.5 ms, respectively, which match well with the ms-scale response in typical biological synapses.[35]

Notably, the memtransistor with a third gate terminal can be used as another presynaptic input for tuning the synaptic plasticity. When the gate bias is swept in a loop at a constant V_{ds} of 1 V in different V_{gs} ranges (**Figure 5**a), huge hysteresis is observed, which is much larger than that of previously reported floating gate transistors for synapse application.[12,14] Typically, the forward sweep causes a more negative threshold voltage (V_{th}) whereas the backward sweep results in a more positive V_{th}. The hysteresis is observed to increase with V_{gs} scan range, with the largest ΔV_{th} reaching 13 V for −10 to 10 V range (Figure 5b). We note that such enormous hysteresis behavior has been consistently observed in our memtransistors of various dimensions (Figure S6, Supporting Information). Factors responsible for the hysteresis behavior in the transfer curves of MoS_2 transistors have been widely studied, including adsorption of gas molecules on the MoS_2 surface, trap states at the interface between MoS_2 and gate dielectric, and defects within the gate stack.[36–41] Particularly, defects in the MoS_2 itself have been found to be an important origin of gate hysteresis, as demonstrated in suspended MoS_2 FETs under vacuum conditions.[42] In our case, the large hysteresis retains when the device is measured in high vacuum (1×10^{-5} mbar), which excludes the absorption/desorption of gas/water molecules as the cause of the gate hysteresis. Besides, we have fabricated control devices on monocrystalline MoS_2 nanosheets with similar gate-stack configuration, and no large hysteresis phenomenon is noticed, indicating negligible charge traps originating from the HfO_2 dielectric. Therefore, it would be reasonable to attribute the observed gate hysteresis to the intrinsic defects in the polycrystalline MoS_2 film.[43] In a most likely scenario, diverse defects (not limited to double sulfur vacancy previously discussed) exist in the atomically thin MoS_2 as a result of sulfur vacancies and grain boundaries. They can introduce a large amount of electron trap states in the band gap of MoS_2. Considering the top-gated device architecture, these trap states will lead to a charge trapping/detrapping process during the V_{gs} scan, and consequently a large hysteresis in the transfer characteristics. Nevertheless, although an in-depth study on the hysteresis behavior is worth being conducted separately, here we will stay focused on its exploration for synaptic devices.

The huge hysteresis behavior in transfer curves enables our MoS_2 memtransistor for analog synapse application by appointing the gate terminal as the presynaptic input for electrical stimulus (Figure 5c). In Figure 5d, at a fixed V_{ds} of 0.5 V, a negative/positive V_{gs} pulse sequence results in a continued increase/decrease in PSC, demonstrating the capability of the device to mimic the LTP/LTD activity of a synapse, respectively. Furthermore, when a higher voltage pulse amplitude is used, the PSC undergoes a faster and larger progressive change due to more traps involved, indicating SADP emulated by the device (Figure S7, Supporting Information). The dynamic response of the synapse to sequences of V_{gs} pulses with different pulse amplitudes are reported in Figure 5e,f. Similar to the response to V_{ds} pulses, a higher negative/positive pulse amplitude leads to a faster potentiation/depression of the synapse. Moreover, the change in PSC due to an opposite pulse polarity over previous pulse sequences is depicted in Figure 5g. Apparently, a larger pulse amplitude can induce a more significant change in PSC for both potentiation and depression processes. Figure 5h shows the synaptic weight change as a function of pulse numbers for different pulse amplitudes. The synapse plasticity gradually increases with increasing pulse number, and finally saturates after a certain number of pulses. Meanwhile, a higher pulse amplitude results in a larger synaptic weight change and a faster saturation, manifesting the SADP characteristic. The response of the artificial synapse shows a dependence on the

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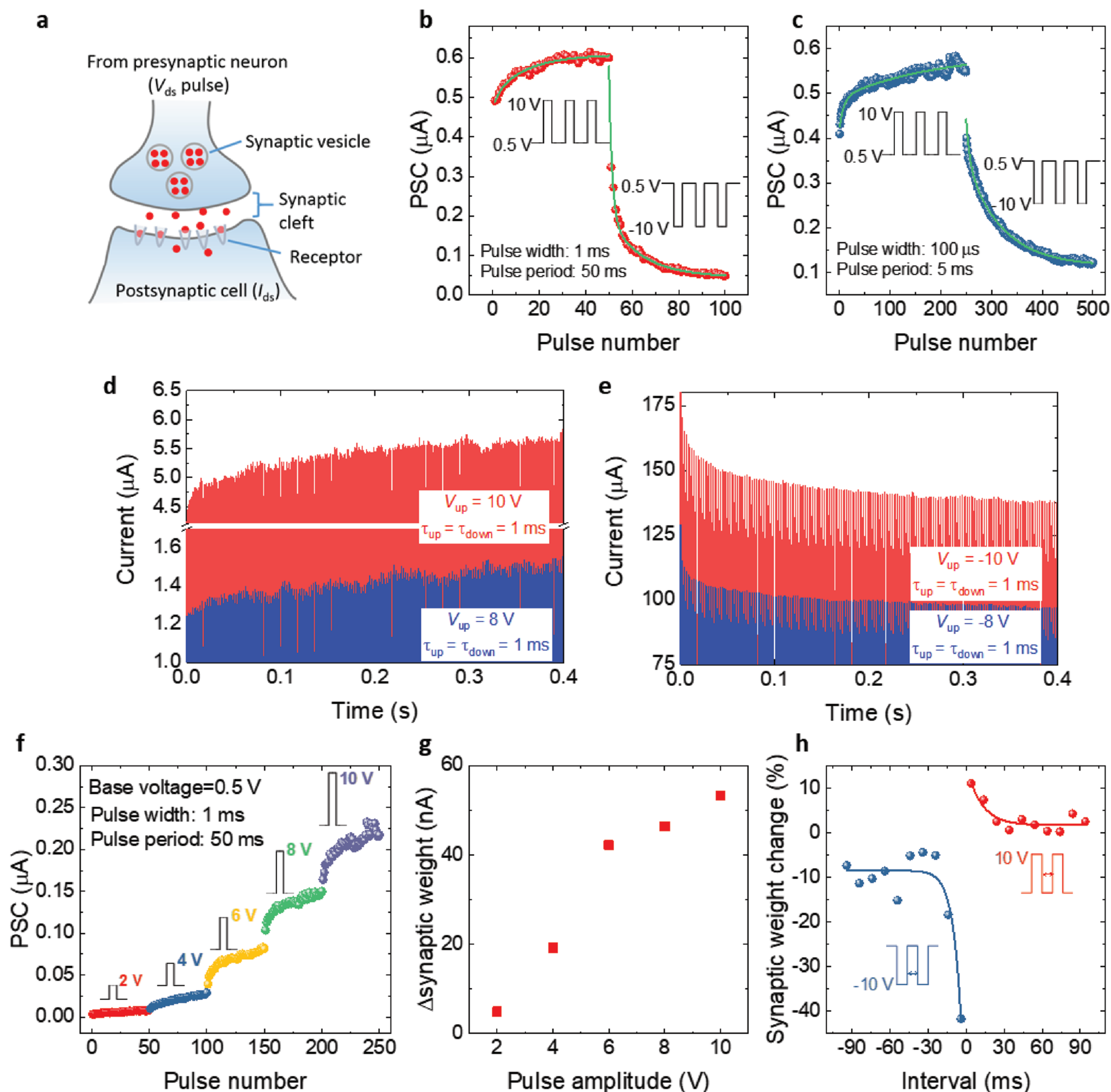

Figure 4. Mimicking the key synaptic activities using the MoS_2 memtransistor with drain terminal serving as the presynaptic input. a) Schematic of the MoS_2-based artificial synapse. Presynaptic excitation is introduced through V_{ds}, while PSC is represented by I_{ds}. b) PSC versus number of pulses on V_{ds}. The application of positive (10 V amplitude) and negative V_{ds} pulse (−10 V amplitude) sequences results in exponential increase and decrease in PSC, manifesting long-term potentiation (LTP) and long-term depression (LTD) process, respectively. 1 ms pulse width and 50 ms pulse period were used. c) PSC versus number of pulses on V_{ds}. 100 µs pulse width and 5 ms pulse period were used. It requires more pulses to generate similar change in PSC due to the shorter pulse width. d) Dynamic response of the memtransistor in response to a sequence of 250 V_{ds} pulses with 10 V (red) and 8 V (blue) pulse voltage, showing progressive synapse potentiation. Pulse width = 1 ms and pulse period = 2 ms. e) Dynamic response of the memtransistor in response to a sequence of 250 V_{ds} pulses with −10 V (red) and −8 V (blue) pulse voltage, showing progressive synapse depression. Pulse width = 1 ms and pulse period = 2 ms. f) PSC versus pulse number with varying V_{ds} pulse amplitude as indicated by segments of different colors. g) Extracted change in PSC after a sequence of 50 pulses for each pulse amplitude, suggesting enhanced potentiation with increasing pulse amplitude. h) Spike-timing-dependent plasticity of the MoS_2 memtransistor. Synaptic weight change dependence on the time interval between paired V_{ds} pulses. The solid lines are exponential fits with time constants of 11.6 ms (red) and 6.5 ms (blue) for positive and negative pulses, respectively.

pulse width and pulse period as well (Figure S8, Supporting Information). In Figure 5i, indirect STDP was mimicked by using paired pulses distanced by a time interval. Positive and negative changes in the synaptic weight are induced using negative and positive pulses, giving rise to 4.8 and 2.7 ms time constant, respectively, which are also well comparable to the

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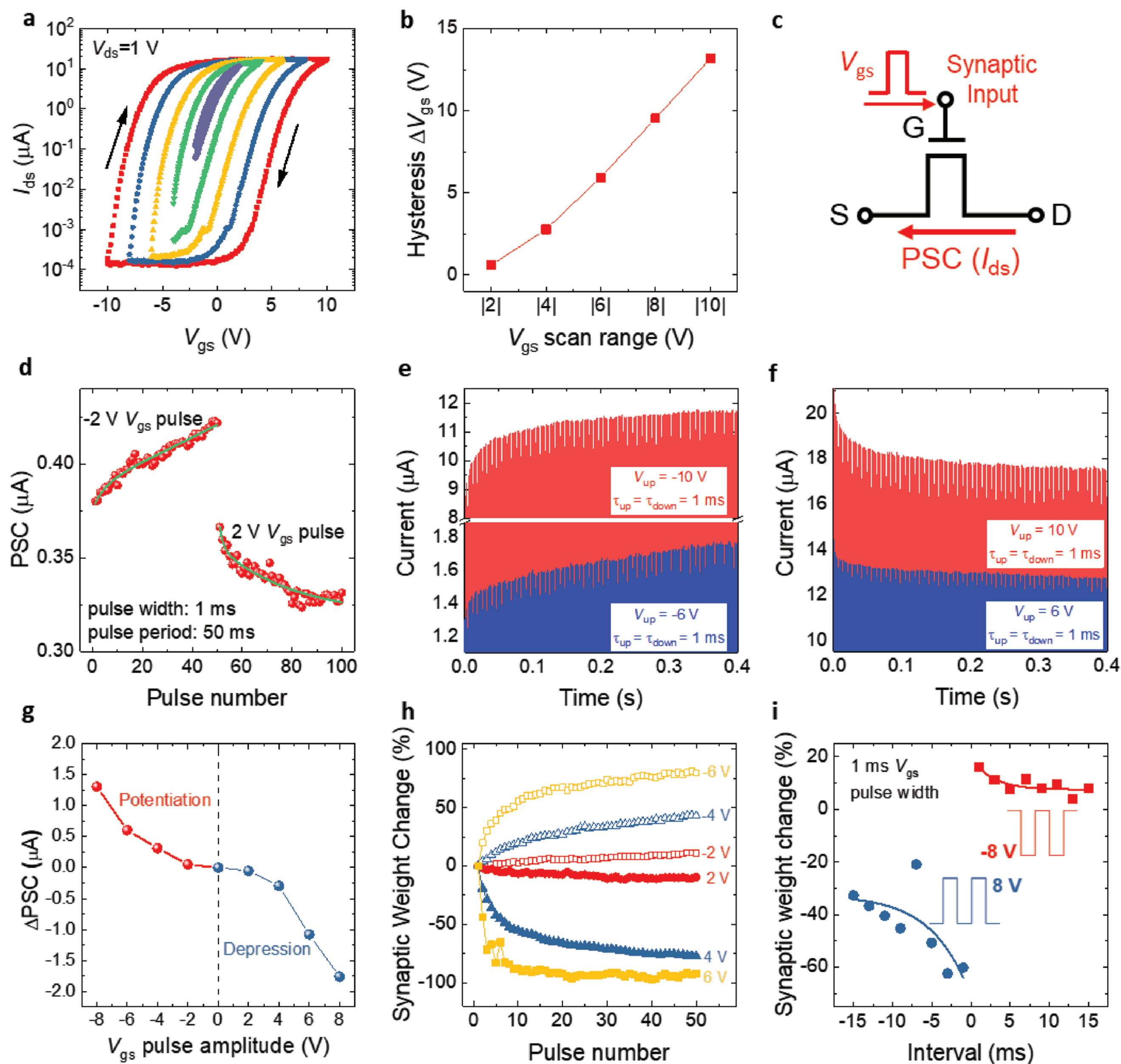

Figure 5. Gate voltage hysteresis of the MoS_2 memtransistor and its synaptic plasticity with the gate serving as presynaptic input. a) Transfer characteristics of the MoS_2 memtransistor, showing hysteresis behavior that increases with V_{gs} sweep range. The sweep direction is indicated by the black arrows. b) Extracted hysteresis in threshold voltage (ΔV_{th}) as a function of V_{gs} sweep range. c) Schematic illustration of the synapse cell with the gate terminal acting as stimulation input. d) PSC versus pulse number for gate pulse trains with pulse amplitudes of ± 2 V. 1 ms pulse width and 50 ms pulse period were used. V_{ds} = 0.5 V was used to read I_{ds}. Negative V_{gs} pulses lead to LTP, while positive V_{gs} pulses give rise to LTD. The solid lines are bi-exponential fittings. e) Dynamic activity of the synapse in response to a sequence of 200 V_{gs} pulses with −10 V (red) and −8 V (blue) pulse amplitude, showing progressive synapse potentiation. Pulse width = 1 ms and pulse period = 2 ms. f) Dynamic activity of the synapse in response to a sequence of 200 V_{gs} pulses with 10 V (red) and 8 V (blue) pulse amplitude, showing progressive synapse depression. Pulse width = 1 ms and pulse period = 2 ms. Additionally, a higher pulse amplitude results in more-efficient potentiation (for negative V_{gs} pulse) and depression (for positive V_{gs} pulse) process. g) Change in PSC (after an opposite V_{gs} pulse is applied), showing apparently an increasing impact with increasing V_{gs} pulse amplitude. h) Positive and negative synaptic weight changes as a function of the pulse number for different pulse amplitudes. i) Spike-timing-dependent plasticity of the MoS_2 memtransistor. Dependence of synaptic weight change on the time interval between paired V_{gs} pulses. The solid lines are exponential fits with time constants of 2.7 ms (red) and 4.8 ms (blue) for negative and positive pulses, respectively. V_{gs} pulses was applied with 0 V base. V_{ds} = 0.5 V was used for current reading.

response times of biological systems. Finally, we emphasize that the flexibility of deploying either drain or gate for presynaptic input distinguishes our analogue synapse from previously reported ones which are usually restrained by single presynaptic input,[14,24] consequently adding another degree of freedom for designing complicated neuromorphic computing systems.

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3. Conclusions

In summary, building on a scalable polycrystalline-MoS_2 thin film, we have experimentally realized a three-terminal memtransistor that exhibits a wide gate-tunability and prominent analog RS behavior with switching ratios as high as $>10^4$. The devices hold promise for synaptic emulators and neuromorphic computing with flexibility in deploying either the gate or drain terminal as the presynaptic input, which can be highly useful for the design of complex brain-like artificial intelligence systems. Furthermore, wafer-scale MoS_2 growth and device fabrication process that are compatible with existing technologies are developed, demonstrating its potential for realizing energy-efficient neuromorphic applications.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

artificial synapses, memtransistor, MoS_2, neuromorphic computing

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