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Monolithically Integrated Flexible Black Phosphorus Complementary Inverter Circuits

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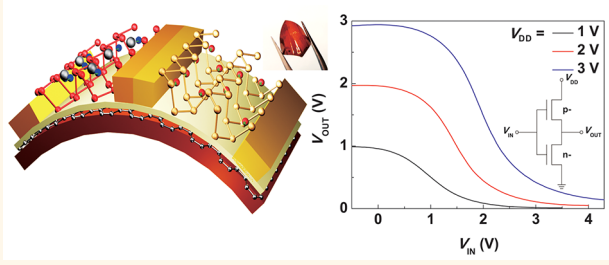
Supporting Information

ABSTRACT: **Two-dimensional (2D) inverters are a fundamental building block for flexible logic circuits which have previously been realized by heterogeneously wiring transistors with two discrete channel materials. Here, we demonstrate a monolithically integrated complementary inverter made using a homogeneous black phosphorus (BP) nanosheet on flexible substrates. The digital logic inverter circuit is demonstrated *via* effective threshold voltage tuning within a single BP material, which offers both electron and hole dominated conducting channels with nearly symmetric pinch-off and current saturation. Controllable electron concentration is achieved by accurately modulating the aluminum (Al) donor doping, which realizes BP n-FET with a room-temperature on/off ratio >10^3. Simultaneously, work function engineering is employed to obtain a low Schottky barrier contact electrode that facilities hole injection, thus enhancing the current density of the BP p-FET by 9.4 times. The flexible inverter circuit shows a clear digital logic voltage inversion operation along with a larger-than-unity direct current voltage gain, while exhibits alternating current dynamic signal switching at a record high frequency up to 100 kHz and remarkable electrical stability upon mechanical bending with a radii as small as 4 mm. Our study demonstrates a practical monolithic integration strategy for achieving functional logic circuits on one material platform, paving the way for future high-density flexible electronic applications.**



KEYWORDS: *flexible, black phosphorus, monolithic integrated, complementary, inverter*

Soft, twisted, stretchable electronic devices have provided an appealing conception to change fundamentally the traditional and predominate hard, rigid, planar integrated chips due to recent advances in materials and process technology.[1−3] Successful outcomes from the pioneering efforts have been consistently demonstrated based on ultrathin inorganics,[4] nanotubes,[5−7] and nanowires,[8] with organic semiconductors[9] being the other potential option. The atomically thin, covalently bonded, and highly ordered crystalline two-dimensional (2D) layered materials (2DLMs) promises further improvements in terms of material, electrical, and mechanical properties, providing advanced capabilities for enabling lightweight, curvilinear, stretchable electronic components and integrated systems on common commodities such as plastics, textiles, and paper.[10−15] An inverter is a 'NOT' logic circuit, which is the nucleus for the logic digital designs. This requires extensive knowledge of the structural and functional characteristics, a particularly important topic that remains less investigated. To date, only a few previous reports have been dedicated to the flexible inverters typically by hybrid integrating two discrete 2DLMs semiconductors with different conducting types together, such as hybrid inverter consisting of one p-type WSe_2 field-effect transistor (FET) and one n-type MoS_2 FET[16] due to the lack of reliable doping technique. Such a heterogeneous complementary inverter is readily formed by a dry transfer or external wiring process. These conceptual circuits can be used to analyze the physical performance of the emerging material and verify the predictive technology, but it will be rather complicated and expensive to handle two kinds of materials for the industrial large-scale high-density device integration. From the engineering standpoint, practical applications for high-density system integration require simple fabrication processes that preferably involve as few materials as possible. Moreover, this inverter focuses mainly on the voltage transfer characteristics, whereas there are voltage overshoots for the dynamic switching behavior; even it is operated at 100 Hz. Complementary inverters based on homogeneous 2D layered materials such as black phosphorus (BP) has not been demonstrated on flexible substrates before. The previous efforts on "*rigid*" substrates to fabricate homogeneous complementary-like inverters have been reported using the same kind of TMDCs material[17,18] as both n- and p-channel depending upon chemical doping in the channel, but the polarity transition is

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relatively unstable and the devices cannot be exposed to air ambience. The alternative technique of homogeneous complementary inverter employs additional gate biases to adjust channel polarities and threshold voltages,[19,20] which adversely makes the device structure and the fabrication process complicated. Several groups have therefore attempted to fabricate homogeneous 2D inverters operated in depletion-load type[10,21] in spite of the drawbacks involving high-power dissipation and low-voltage gain.

Black phosphorus is by far the only monoelemental 2D layered semiconductor[22] that exhibits superior mechanical flexibility originating from its puckered crystal structure, with Young's modulus (zigzig, 0.166 TPa; armchair, 0.044 TPa)[23] 1 order of magnitude smaller compared to that of graphene (1.0 TPa)[24] and MoS_2 (0.33 TPa).[25] These attractive attributes are envisioned to be a competitive alternative for flexible electronics applications. Undoped BP shows p-type conducting behavior with hole mobility as high as 6000 $cm^2\ V^{-1}\ s^{-1}$ at a low temperature of 0.3 K.[26] Moreover, the conductivity type control in BP can be modified by forming covalent bonds with foreign dopants, benefiting from the existence of the dangling bonds on its surface.[27−30] For example, a previous study from our group has recently demonstrated theoretically and experimentally that aluminum (Al) atoms are an efficient electron donor species for BP, with the n-BP FETs displaying up to 2.5 times enhanced electron mobility (105 $cm^2\ V^{-1}\ s^{-1}$ on SiO_2/Si at room temperature).[31] This offers levels of performance exceeding that of n-MoS_2 (1−50 $cm^2\ V^{-1}\ s^{-1}$),[32,33] thus allowing technologies that require both p- and n-type semiconductors to be implemented, such as a p−n homojunction for near-infrared photovoltaics. However, the devices in that work including both the transistors and the p−n homojunction diode were demonstrated on rigid SiO_2/Si rather than flexible substrates. Even if the device fabrication process on rigid substrates is mature enough for industrial large-scale fabrication, it cannot be transferred directly to the flexible electronic applications. Moreover, the precise tunability of carrier concentration in BP has yet to be realized by dopants doping, which hinders the demonstration of systems integrated by devices with balanced electrical properties.

In this work, we address the next key challenge in the development of flexible electronics by realizing the monolithic integrated complementary inverter made entirely using a homogeneous BP nanosheet on flexible polyimide (PI) substrates. The digital logic inverter circuit is based on the development of threshold voltage tuning in a single BP nanosheet, which offers both electron and hole dominated conducting channels with nearly symmetric pinch-off and current saturation. We show that an n-FET with a room-temperature on/off ratio $>10^3$ and controllable carrier concentration can be achieved by accurately modulating the Al atoms doping. Simultaneously, work function engineering is employed to obtain a low-potential-barrier electrode that facilities hole injection, thus enhancing the current density of the p-FET by 9.4 times. The flexible inverter circuit shows clear digital logic voltage inversion operation, along with a direct current (DC) voltage gain, exhibits alternating current (AC) dynamic signal switching at a record high frequency up to 100 kHz, and presents remarkable electrical stability upon mechanical bending. Our studies clearly take the functionality and complexity of the van der Waals layered materials to the next level by establishing a monolithic integration platform technology on flexible substrates, which is nontrivial to future high density logic circuit applications, such as bendable flat panel displays and wearable identification tags.

RESULTS AND DISCUSSION

By patterning the surface of BP prior to exposure to the Al atoms dopants, spatially controlled electron doping profiling along the length of BP can be achieved, as discussed in detail in our previous study.[31] To take a further step, the precise tunability of the dopants concentration enables us to modulate the electron concentration as well as the threshold voltage, as shown in Figure 1a. The thickness of the BP flakes used here

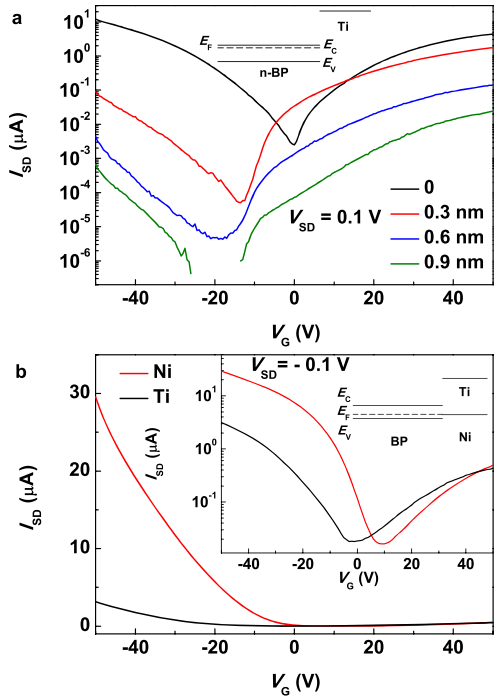

Figure 1. Tuning the threshold voltage and polarity of BP transistor by dopants doping and metal contact engineering. (a) Transfer characteristics of Al-doped BP FET as a function of the quantity of the Al dopants. It is observed that the threshold voltage shifts negatively with increasing the dopants, and the source−drain current decreases consecutively, indicative of the enhanced electron doping in the BP channel. The inset shows the energy level diagram. (b) Comparison of the transfer curve of Ni-contacted FET with that of Ti-contacted one. These two FETs are fabricated on one single BP sheet. As the work function of Ni (5.15 eV) is higher than that of Ti (4.33 eV), it is observed that the threshold voltage shifts positively from 0 to ∼9 V, showing that Ni contacts facilitate holes injection and transport in the undoped BP, resulting in low contact resistance between the electrodes and the undoped BP sheet. The inset shows the energy band diagram using Ti and Ni electrodes.

was <10 nm as measured by AFM (Figure S1, Supporting Information), and the substrates are degenerately doped p-Si capped with 300 nm thermal dioxide. The pristine device displayed typical p-type behavior with the source−drain current for $V_G < V_{TH}$ (V_{TH}, threshold voltage) higher than that for $V_G > V_{TH}$. Upon the Al atoms doping step (for experimental details, see ref 31), it is observed that the threshold voltage of the transistors was negatively shifted in a continuous manner over a wide range from 0 V to ∼−20 V, and the transfer curve of the transistor changed to yield typical n-type characteristics. Ti metal is utilized as the electrodes for Al-doped n-FETs, and the

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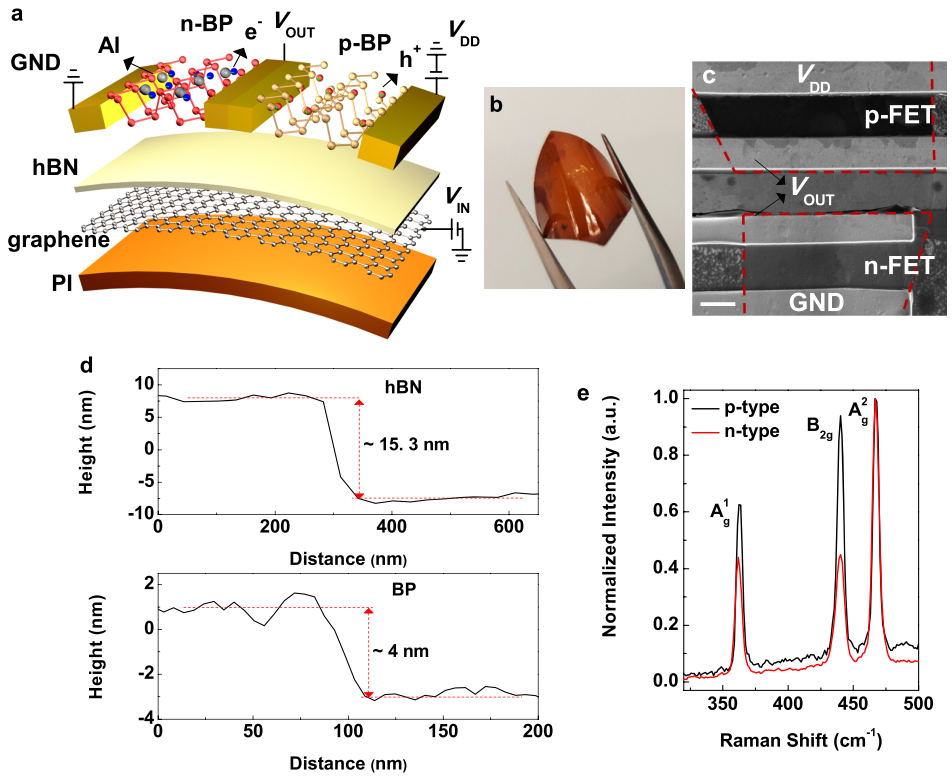

Figure 2. Schematic and structural characterization of the homogeneous BP based complementary inverter on the flexible PI substrate. (a) 3D schematic diagram of the flexible BP complementary inverter comprising Al-doped n-BP transistor and undoped p-BP transistor (not to scale). Graphite and hBN were used as the back gate and gate dielectric layer, respectively. Ti/Au and Ni/Au were used as the electrodes for n- and p-type transistors, respectively. (b) Photograph of the inverter circuit fabricated on highly bendable PI substrate when it is handled by the tweezers. (c) Scanning electron microscopic image of the inverter, showing a pair of n- and p-FETs on a single BP sheet. Scale bar, 2 μm. The red dashed lines show the area of the BP sheet. The spacing between the metal fingers is ~2.6 μm, and the finger width is ~1.7 μm. (d) Topological line profile of the hBN (top panel) and BP (bottom panel) sheet, presenting their thicknesses to be ~15.3 nm and ~4 nm, respectively. (e) Raman spectra for n- and p-type BP segments with 532 nm laser excitation incident in the z direction. The peak positions of all three modes (A_g^2, B_{2g}, and A_g^1) do not change, but the relative intensities of A_g^1 and B_{2g} for Al-doped n-type BP decrease significantly as compared with that of the undoped one.

output plots (Figure 3b) indicate that low work function Ti (4.33 eV) exhibits linear output characteristics with n-BP and facilitates electron transport, as schematically described by the band diagram illustrated in the inset of Figure 1a. Our doping mechanism differs from the chemical doping that previous literatures[17,18] used for polarity transition of TMDCs. We n-dope the BP channel by thermal diffusion of Al atoms, and the dopants diffuse into the intercalated sites of the BP crystal lattice, donating electrons to convert the BP segment from p- to n-type.[31] However, the dopants introduced by chemical doping lie at the surface of the host channel, and the polarity transition is demonstrated by surface charge transfer. The chemical doping is unstable, and the devices cannot be exposed to air ambient. Furthermore, it is difficult for them to control the doping concentration in the MoS_2 *via* the chemical doping method because the effective dopants are resolved in the solution,[17] and the solution dropping method is not compatible with the high-density device integration. Because the Al atoms used in our work are deposited by an atomic layer deposition (ALD) system, the quantity of the Al atoms can be extraordinarily precise by controlling the carrier gas flow of the trimethylaluminum (TMA) precursor. We can choose accurately the appropriate doping dose to precisely control the doping level, which is also one of the significant technological advances of this work.

Figure 1b shows the comparison of the transfer curves between Ni- and Ti-contacted back-gated undoped BP FETs, which are fabricated from a single pristine BP sheet with a thickness of ~11.3 nm (Figure S2, Supporting Information). It is observed that the threshold voltage shifts positively from ~0 V for Ti-contacted transistor to ~9 V for Ni-contacted one, and the ON state conductance at V_G = −50 V was improved 9.4 times by Ni contacts. Ni contacts exhibit linear I_{SD}−V_{SD} characteristics in terms of V_G (Figure S3, Supporting Information), which is attributed to the low barrier height of Ni with undoped BP, as schematically shown in the inset of Figure 1b, where the work function of undoped BP is 5.16 eV.[34] The Ni metal with a large work function (5.15 eV) tends to line-up with the valence band of the pristine BP and provides efficient hole injection from the metal electrode into the undoped BP channel due to a low hole Schottky barrier height. This makes the Ni electrode an ideal material for demonstrating high-performance p-type BP FETs. On the other hand, the band level of Ti is aligned to the conduction band of undoped BP, resulting in a high barrier height for hole injection in pristine BP (inset of Figure 1b, and Figure S3a, Supporting Information). As the total resistance (R_T) of the FET can be written as $R_T = R_C + R_{CH}$, where R_C is the contact resistance and R_{CH} is the channel resistance. We can extract that the contact resistance for undoped BP is reduced by 28 kΩ by employing Ni contacts as compared to that of Ti contacts. We

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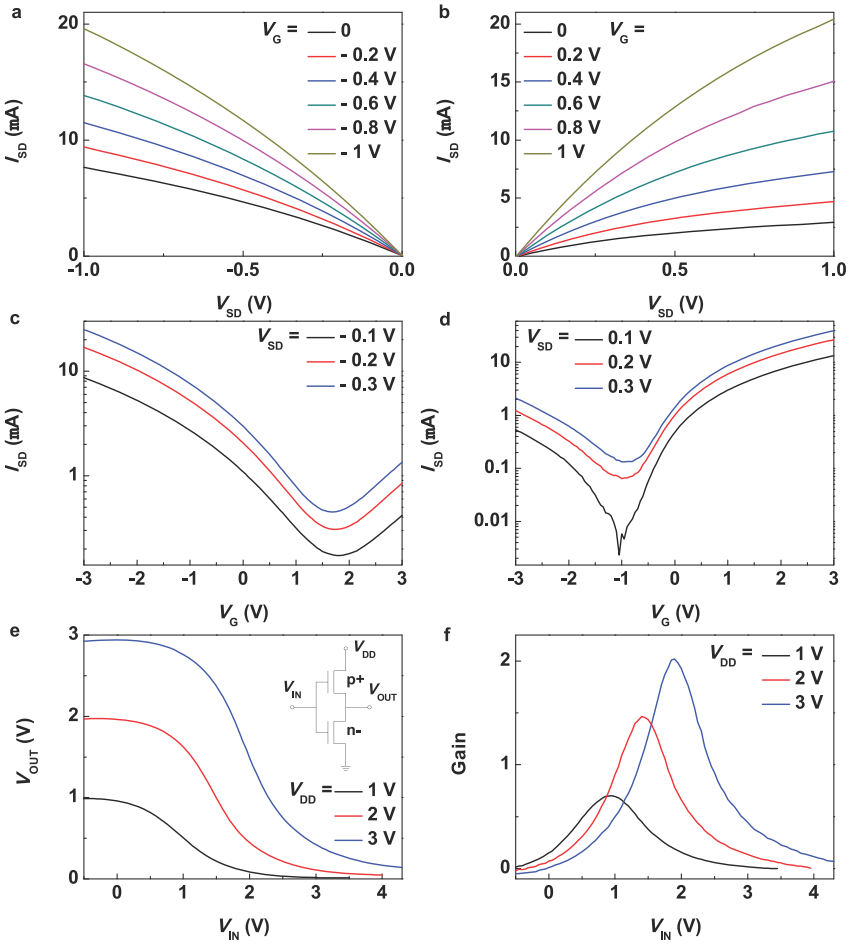

Figure 3. Electrical properties of the flexible homogeneous BP complementary integrated digital inverter. I_{SD}−V_{SD} output characteristics in terms of V_G for (a) the p-type and (b) n-type BP FETs. $|V_G|$ varies from 0 to 1 V in steps of 0.2 V, from bottom to top. Transfer curves (I_{SD}−V_G) at different source−drain bias voltages for (c) the p-type and (d) n-type BP FETs. V_{SD} = 0.1, 0.2, and 0.3 V. (e) V_{OUT}−V_{IN} characteristics of the inverter operated at V_{DD} = 1, 2, and 3 V. The inset shows the circuit scheme of the complementary inverter. (f) Voltage gain (−dV_{OUT}/dV_{IN}) as a function of input voltage V_{IN}. The maximum gain is ∼2 with a threshold voltage of 2 V at V_{DD} = 3 V.

also analyzed the contact resistance using a geometry-based analytical model[35] and extracted the R_C for Ti and Ni electrodes to be ∼37800 Ω and ∼3133 Ω from the simulated I_{SD}−V_G curve (see S5 in the Supporting Information), respectively, which is on the same order with the experimental value of 28 kΩ. The control of the majority carrier type in a BP channel, that is, electron (n-type) or hole (p-type), is demonstrated here by dopants doping and metal contact work function engineering. The continuous modulation of the threshold voltage along with the on/off current offers the technique to achieve best matching of electron and hole transport in both n- and p-type FETs with the same channel dimensions.

Next, flexible complementary inverter with a back-gate geometry is demonstrated on PI substrate using a single BP sheet comprising both p-type and n-type channels (see Methods for details). Figure 2a shows the three-dimensional (3D) schematic of the van der Waals inverter circuit structure, in which hexagonal boron nitride (hBN) and graphene were integrated as the dielectric and gate layer, respectively. Since phonon scattering and roughness scattering can severely degrade the mobility in BP, the clean and atomically smooth surface of hBN can screen the scattering and enhance the mobility of BP transistors, which is superior to those supported on SiO_2. PI films are utilized as the flexible substrate because of their high Young's modulus (∼3.5 GPa), thermal stability (glass transition temperature ∼410 °C), and solvent resistance, which are compatible with the standard device fabrication process and enable us to demonstrate highly bendable devices (Figure 2b). Figure 2c shows a scanning electron microscopy (SEM) image of the top view of the vertically stacking BP/h-BN/graphene inverter circuit, which clearly highlights the BP channel, Ti/Au metal contacts for n-type transistor, and Ni/Au metal contacts for p-type transistor. The channel width is ∼2.6 μm, and the metal finger width is ∼1.7 μm. The p- and n-channels are spatially separated by etching away the intermediate segment to prevent current leakage. It is worthy to note that the two FETs are fabricated side-by-side on the same BP sheet, which is clearly superior to the schemes employing two different materials such as BP p-FET and MoS_2 n-FET.[36] This is because the assemble capacity limitation will be the most critical bottleneck to fabricate a high-density inverter circuit, which hinders it for practical application in high-density logic circuits. Topological line profiles (Figure 2d) measured by atomic force microscope (AFM) show the thicknesses of hBN and BP sheet to be ∼15.3 nm and ∼4 nm, respectively. The Raman spectra of the BP, as depicted in Figure 2e, show three BP phonon peaks around 361.7, 439.9, and 467.0 cm^{-1},

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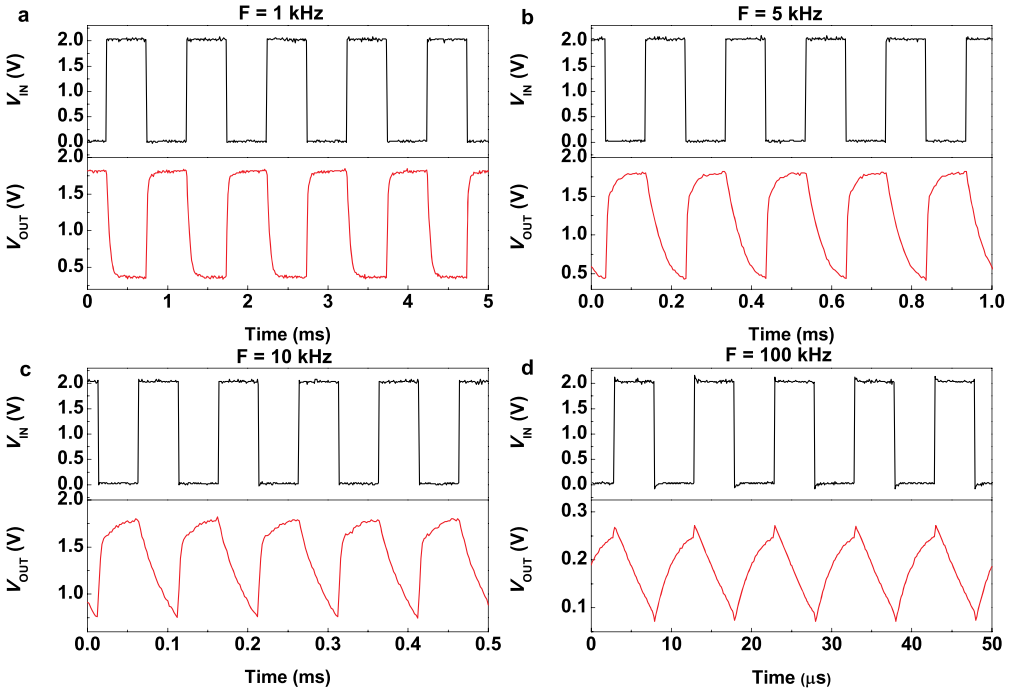

Figure 4. Dynamic switching capability of the flexible homogeneous BP complementary inverter. Plot of input voltage V_{IN} and output voltage V_{OUT} *versus* time at a frequency of (a) 1, (b) 5, (c) 10, and (d) 100 kHz for the inverter circuit. The supply voltage, V_{DD} = 2 V. V_{IN} was a square wave signal with minimum and maximum values of 0 and V_{DD}, and it causes the output voltage to oscillate synchronously with a phase difference of π.

corresponding to the A_g^1, B_{2g}, and A_g^2 vibration modes, respectively.[37,38] The relative intensities of A_g^1 and B_{2g} for doped segment decrease significantly as compared with that of undoped one, but we did not observe the measurable frequency shifts. While a more detailed discussion of the peak intensity dependence on the dopants doping is not the focus of this work, the Raman measurements may reflect the dopants-induced lattice distortion that has been recently theoretically predicted by density functional theory (DFT) calculations.[31]

Gate-modulated output characteristics of both FETs are depicted in Figure 3a,b, which illustrate the almost symmetric $I_{SD}-V_{SD}$ curves for the pair of p- and n-FETs under various gate voltages ranging from 0 to 1.0 V in steps of 0.2 V. The $I_{SD}-V_{SD}$ curves show linear behavior at low source-drain voltages, suggesting the formation of a low potential barrier at the interface between the selected metals and BP. The transfer characteristics are shown in Figure 3c,d, presenting that the carrier injection efficiency is at the same level for both FETs. The threshold voltage V_{TH} shifts negatively from 1.8 V for p-FET to −1 V for n-FET. From n-FET at V_{SD} = 0.1 V, we recorded a maximal on-current of 13.37 μA (3.82 μA/μm) and an off-current of 2.3 nA, resulting in a current on/off ratio of 5.8×10^3 in the ±3 V back-gate voltage range. The room-temperature electron field-effect mobility of 83.8 $cm^2\ V^{-1}\ s^{-1}$ at a drain voltage of V_{SD} = 0.1 V can be extracted using the expression $\mu = (dI_{SD}/dV_G) \times [L/(W \times C_0 \times V_{SD})]$, where L is the channel length, W is the channel width, $C_0 = 2.26 \times 10^{-3}$ F cm^{-2} is the back-gate capacitance per unit area ($C_0 = e_0 e_r/d$; $e_0 = 8.85 \times 10^{-12}$ Fm^{-1}; $e_r = 3.9$;[39,40] d = 15.3 nm). The n- and p-type BP FETs show nearly symmetric electronic behavior and simultaneously high performance, including saturation current >17 μA at V_{SD} = 0.2 V (26.7 μA for n-FET vs 17 μA for p-FET) and high peak transconductance (13.2 μS for n-FET vs 7.7 μS for p-FET; see Figure S5, Supporting Information).

The digital circuit diagram of the inverter is depicted in the inset of Figure 3e, where the supply voltage, input voltage, and output voltage are labeled as V_{DD}, V_{IN}, and V_{OUT}, respectively. An inverter is a 'NOT' logic circuit that outputs a voltage representing the opposite logic level to its input. The quality of a logic inverter is often evaluated using its voltage transfer curve, which is a plot of input voltage *versus* output voltage, as shown in Figure 3e. Clean inverter action is observed for switching between logic '1' (close to V_{DD}) and logic '0' (close to 0 V). When V_{IN} is close to 0 V (logic state '0'), the n-FET is nonconducting, and V_{OUT} is approaching the supply voltage V_{DD} (logic state '1'). When V_{IN} is pulled up to a high voltage (logic state '1'), V_{OUT} decreases to near 0 (logic state '0'), indicative of the complete rail-to-rail signal inversion. For example, when the V_{DD} = 1 V, the highest output voltage is 0.99 V, which approaches the V_{DD}, and the lowest output voltage is 0.01 V, which approaches 0 V, indicating that one transistor of the pair is off, therefore suggesting "complementary" operation. The switching current (Figure S6, Supporting Information) is observed to have a peak for all voltage ranges, confirming the complementary nature of the circuit operation. The slope of the transition region in the middle provides a measure of the voltage gain (defined as $-dV_{OUT}/dV_{IN}$), which presents the sensitivity of V_{OUT} to the change in V_{IN}. A larger-than-unity voltage gain is achieved even under low supply voltage V_{DD} of 2 V (as shown in Figure 3f), indicating that our inverter can serve as the basis for multistage logic circuits. A gain higher than 1 is desired for cascade logic application because it makes the circuit regenerative and robust to errors, while further improvements are expected from downscaling the gate dielectric thickness to improve the subthreshold swing of the transistors due to a better electrostatic control. Another possible approach includes reducing the contaminants and bubbles at the graphene/hBN and hBN/BP van der Waals heterointerfaces by optimizing the

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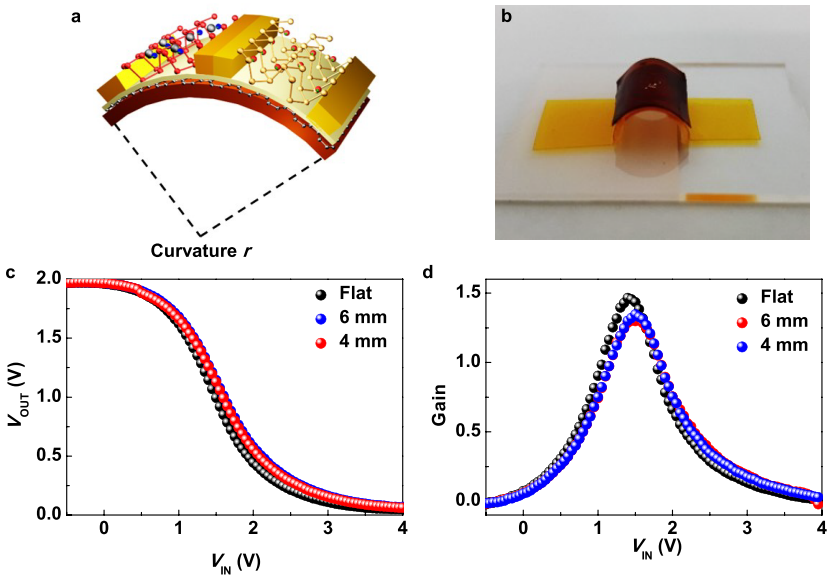

Figure 5. Mechanical bending test of the inverter circuit. (a) Schematic of the bent device structure; r is the curvature radius. (b) Photographic image of the bent device on a bending tester with a radius of 4 mm. Scale bar, 8 mm. (c) V_{OUT}−V_{IN} and (d) voltage gains of the flexible inverter before bending and after bending at different radii of curvature r. No significant degradation is observed under mechanical bending. The voltage gain is still higher than 1, thus supports its functionality.

device fabrication process, such as using the PPC/PDMS (PPC, poly(propylene carbonate)) hot pick up technique, followed by high-temperature annealing in forming gas atmosphere. This is expected to reduce the interface states density, thus allowing the transistors to achieve an improved subthreshold swing. The electrical properties of the transistors and the inverter are similar to the control sample on the SiO_2/Si substrate (Figure S7, Supporting Information), indicating that the fabrication process is compatible with the flexible devices. We can observe the mismatch between input and output voltage level, which is one drawback of the nascent conceptual inverter circuit. This is due to the small transconductance and the small back-gate capacitance, which can be addressed by further downscaling the gate dielectric thickness.

Another important figure-of-merit for an inverter circuit is the switching frequency, which determines the dynamic performance of the system. In particular, there is a strong need to construct a dynamic controller instead of static controller in order to achieve dynamical behavior of state response. Our inverter is switched by a square voltage waveform applied on the gate, which causes the output voltage to oscillate synchronously with a phase difference of π, as shown in Figure 4. The supply voltage V_{DD} is 2 V, and the input voltage V_{IN} was a square wave signal with minimum and maximum values of 0 V and V_{DD}. Figure 4 shows the time domain plots at four frequencies (1, 5, 10, and 100 kHz). At 1 kHz frequencies, the output voltage waveform of the inverter retains well, and no over/undershoot of output voltage was observed, which has outperformed the results measured from the flexible inverter consisting of one WSe_2 p-FET and one MoS_2 n-FET.[16] The switching speed of their device is limited to <100 Hz by the ion conductivity of the electrolyte gate dielectric, severely reducing its utility for the dynamic controller circuit. The AC dynamic signal operation of our inverter is demonstrated at frequencies up to 100 kHz, which is the record high speed for a 2D complementary inverter. It is comparable to that of p-BP/n-MoS_2 inverter circuits reported by Su *et al.*,[41] who assembled the inverter circuit by externally wiring two discrete FETs on rigid substrates, which is superior to that of the inverter based on α-$MoTe_2$ p-channel and MoS_2 n-channel on glass.[42] It is observed that the voltage gain decreases with increasing frequency. This is because the influence of high parasitic capacitances and fringing fields can be mitigated by further circuit engineering and by improving the device transconductance.

Reliable mechanical bendability is required for flexible electronic applications. To evaluate the mechanical reliability of the flexible complementary inverter, it is subjected to mechanical bending at different radii of curvature in the channel transport direction. A schematic of the bending condition is shown in Figure 5a, in which r is the curvature radius. And Figure 5b presents the real photograph of the custom-designed bending measurement fixture showing the device under bending condition (r = 4 mm). The induced tensile strain of our device was calculated by $\varepsilon = t_s/(2r)$, where t_s is the overall thickness of PI substrate. For our device, t_s = 60 μm, and the bending radius was 4 mm (or 6 mm), which corresponds to tensile strain up to 0.75% (or 0.5%). Figure 5c shows the voltage transfer curves of the inverter before bending and after bending at curvature radius of 6 mm and 4 mm. Importantly, no significant electrical degradation is observed from the voltage transfer characteristics, indicating excellent electrical stability upon mechanical bending. The maximum voltage gain remains to be higher than 1 at V_{DD} = 2 V and is virtually insensitive to the applied tensile strains up to 0.75%. These results indicate that the van der Waals device can handle the applied mechanical strains even at a bending radius of 4 mm. The essential ingredients of our inverter circuit are the ubiquity of the n-channel BP FET operation previously thought to show only p-channel behavior, the accurate modulation of threshold voltage by effective Al doping technique, the capability to construct functional multistage logic circuits, the record high switching speed among the 2D complementary logic circuits, and the reliable flexible performance. The performance of our flexible, homogeneous BP inverter circuits is thus promising for a broad range of logic circuit applications such as the driving

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circuit of flexible active-matrix e-paper displays or identification tags.

CONCLUSIONS

In conclusion, we have demonstrated effective threshold voltage tuning in BP transistors by accurately controlling the Al-donors doping, whereas the drive current of p-FET is enhanced by high work function Ni contacts. This enables us to fabricate robust complementary inverter logic circuit based on a single BP nanosheet on highly flexible substrate. The inverter circuit shows significant rail-to-rail voltage inversion operation with a larger-than-unity gain and simultaneously exhibits a record high dynamic voltage switching frequency up to 100 kHz. The inverter circuit is also able to retain original characteristics even when bended to a radius of curvature as small as 4 mm. Our study demonstrates the feasibility to implement van der Waals vertically stacked devices for practical digital logic functions. This is fundamentally superior over the previously reported heterogeneous inverters involving two discrete FETs connected through external wiring. Our monolithic inverter presents an important step toward the development of flexible logic circuits with a high potential for a broad range of applications including the driving and switching circuits for bendable flat panel displays and wearable identification tags.

METHODS

Fabrication of the Flexible Homogenous BP Inverter Circuit. Commercially available polyimide (PI) sheets with a thickness of ∼60 μm (Polyonics) were adopted as the substrate. A layer of SU-8 photoresist was spin-coated, followed by curing process to smoothen the flexible PI substrate to ∼0.3 nm surface roughness before fabricating devices on it. The inverter consists of a graphene bottom gate, a hexagonal BN (h-BN) gate dielectric (∼15.3 nm thick), and a single BP sheet (∼4 nm thick) for both the p- and n-channels. Graphene was mechanically exfoliated from kish graphite onto the substrate, followed by stacking of h-BN and BP flakes consecutively in two dry transfer steps using poly(dimethylsiloxane) (PDMS) stamps. Exfoliation of BP and subsequent fabrication procedures where BP was unprotected (for example, uncovered with PMMA or Al_2O_3) were performed in an argon-filled glovebox with an O_2 and H_2O concentration <0.2 ppm. The electrodes were fabricated by the standard electron beam lithography followed by electron beam evaporation of Ti/Au (Ti/Au, 60/90 nm) for n-type FET and sputtering of Ni/Au (Ni/Au, 10/140 nm) for p-type FET, respectively. A second step of electron beam lithography defined a local area covering the BP region to be Al-doped. Subsequently, Al (∼0.3 nm thick) and Al_2O_3 (∼15 nm) layers were deposited at 120 °C by an atomic layer deposition (ALD) system with its vacuum chamber attached to an argon-filled glovebox (precursor: trimethylaluminum and water). Then, CHF_3-based deep reactive-ion etching (RIE) process was used to remove the BP segment between the p- and n-channels to prevent leakage currents.

Electrical Characterization. All electrical measurements were performed in the dark in a closed cycle cryogenic vacuum probe station (∼10^{-6} mbar) at room temperature. The quasi-static measurements were conducted using a semiconductor parameter analyzer (Keithley 4200-SCS). The dynamic characterizations were performed using a digital waveform generator (Hewlett-Packard 33120A) as the input source and a digital oscilloscope (Rigol DS1062C, input impedance 1 MΩ) for the output signal detection. For static bending, the flexible inverter circuit is attached onto the surface of rigid cylinders with predefined radius (r = 6 mm and 4 mm).

Materials Characterization. Raman spectra were measured in the backscattering configuration. The scattered light was analyzed on a Witec Alpha 300R confocal microscope spectrometer using a 100× objective lens with about ∼1 μm beam spot diameter and 1800 lines per mm grating with about 1.236 cm^{-1} spectral resolution. The excitation light source is a 532 nm laser operating at 1 mW. No polarized analyzer was used, so that light polarized both perpendicular and parallel to the scattering plane was collected. The spectrometer integration time was 1 s for all measurements. Atomic force microscope scans were acquired using a Bruker Dimension FastScan microscope operated in the tapping mode. Between the scans, the BP samples were kept under atmosphere in a class 1000 clean room with controlled 50% relative humidity. The nanostructure and morphology of the inverter were characterized by field-emission scanning electron microscopy (FEI, Verios 460).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.7b03703.

Table S1: Properties of published inverters based on 2D layered materials. Figures S1−S7: Materials and characterization, additional experimental details (PDF)

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K.-W.A. supervised the project. Y.L. carried out the experiments.

Notes

The authors declare no competing financial interest.

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