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Wafer-Scale 2D Hafnium Diselenide Based Memristor Crossbar Array for Energy-Efficient Neural Network Hardware

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Memristor crossbar with programmable conductance could overcome the energy consumption and speed limitations of neural networks when executing core computing tasks in image processing. However, the implementation of crossbar array (CBA) based on ultrathin 2D materials is hindered by challenges associated with large-scale material synthesis and device integration. Here, a memristor CBA is demonstrated using wafer-scale (2-inch) polycrystalline hafnium diselenide ($HfSe_2$) grown by molecular beam epitaxy, and a metal-assisted van der Waals transfer technique. The memristor exhibits small switching voltage (0.6 V), low switching energy (0.82 pJ), and simultaneously achieves emulation of synaptic weight plasticity. Furthermore, the CBA enables artificial neural network with a high recognition accuracy of 93.34%. Hardware multiply-and-accumulate (MAC) operation with a narrow error distribution of 0.29% is also demonstrated, and a high power efficiency of greater than 8-trillion operations per second per Watt is achieved. Based on the MAC results, hardware convolution image processing can be performed using programmable kernels (i.e., soft, horizontal, and vertical edge enhancement), which constitutes a vital function for neural network hardware.

1. Introduction

With the rapid rise of big data and artificial intelligence, alternative computing hardware for beyond-CMOS electronics is required to circumvent challenges associated with power consumption and data transport latency.[1,2] Electronic synapses and their artificial neural networks (ANNs) are imperative to overcome the power consumption limitation in conventional von Neumann architecture due to their superior energy and area efficiency by mimicking human neurons, synapses, and their networks.[3,4] Memristors are known as promising candidates for artificial synapses, constituting a key building block for neuromorphic computing. Moreover, crossbar array (CBA) made of memristors is promising to construct neural networks due to its fast and highly parallelized computing capability that utilizes multiply-and-accumulate (MAC) operation based on Ohm's law and Kirchhoff's law.[5,6] However, state-of-the-art memristive CBA using transition metal oxide (TMO) is suffering from challenges such as limited resistive switching (RS) ratio and considerable temporal (cycle-to-cycle) and spatial (device-to-device) variability,[7–9] which necessitates alternative material platforms with better switching reliability.

Memristors based on 2D materials have emerged as a promising option over TMO-based memristors[10,11] due to their unique properties and superior device performance, including large RS ratio,[12] low switching voltage,[12,13] small device variation,[14] as well as, capability of transition between the threshold and bipolar RS.[12,15] However, conventional 2D material-based memristive devices are fabricated using mechanical exfoliation, which lacks a good control of flake thickness and poor spatial variation.[16–19] Moreover, due to the single crystallinity of the exfoliated flake, post-treatments are required to decorate defects for creating switching pathways, such as, ion and electron beam irradiation, which hinder the implementation of circuits and computing hardware.[15,20–22] To address these inherent limitations caused by mechanical exfoliation, considerable efforts have been dedicated to develop scalable fabrication processes. One such approach is liquid-phase exfoliation and spin-coating, which can produce large quantities of materials, but at the expense of crosspoint area scaling and nanoflake orientation control, resulting in poor endurance and low array density.[23–25] Another scalable approach is wafer-scale 2D material synthesis that by far has been primarily driven by logic applications which demand monolayer, high mobility, and single crystallinity.[26,27] Recently, memristors based on chemical vapor deposition (CVD) grown 2D materials with intrinsic defects have been demonstrated with the potential for wafer-scale device fabrication capability with low device

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variation.[14] However, this transfer method can introduce a high density of wrinkles and chemical residuals on the transferred films, which varies the effective area and thus the resistance of the switching medium.[14,25] Moreover, the switching voltage of such devices is deemed too high (≈3 V), which could hinder its application in energy-efficient computing. Furthermore, only statistical analysis of standalone devices was performed, and CBA-based circuits for neural network hardware were not reported. To exploit 2D material-based memristive CBA for next-generation computing hardware, it is essential to develop controllable material growth and clean transfer technique, in addition to robust and scalable process integration.

Hafnium diselenide ($HfSe_2$) is a 2D semiconductor with indirect bandgap, and variable resistive states have been reported in $HfSe_2$-metal compounds, manifesting its potential for memristive devices.[28,29] Moreover, most $HfSe_2$-based electronic devices are fabricated by exfoliated flakes due to the challenges associated with large-scale growth and fabrication.[29,30] In this work, a memristive CBA based on $HfSe_2$ is fabricated and implemented in neural network hardware. The 2D polycrystalline $HfSe_2$ is grown by molecular beam epitaxy (MBE) with a controllable and uniform growth on wafer-scale substrate. A chemical-free metal-assisted van der Waals (vdW) transfer method is developed, which overcomes the stability issue of $HfSe_2$ in ambient conditions.[31] Building on such a platform, memristive CBA with a low switching voltage and energy consumption is demonstrated. The RS mechanism relies on conductive metal filaments driven by external voltage bias and exhibits a strong dependence on defect density and electrode materials. Moreover, the devices possess analog synaptic weight transition with large switching ratio, resulting in high image recognition accuracy in ANN. Hardware implementation of neural networks is achieved based on the CBA, such as accurate and energy-efficient MAC operation and programmable convolutional image processing operation, manifesting the potential of 2D material-based memristors for next-generation neural network hardware.

2. Results and Discussion

2.1. Wafer-Scale Synthesis of Polycrystalline Hafnium Diselenide Thin Film

The qualities of as-grown 2D-material thin films vary with different substrates due to the difference of adatom diffusion constant,[32] existence of substrate dangling bonds,[33] and the guide effect coming from the atomic orientation of substrates.[34,35] Usually, the growth on single-crystal substrate with similar lattice structure results in high crystal quality and the same orientation as the substrate. Inspired by such phenomena, we intentionally choose an amorphous substrate (SiO_2/Si wafer) to synthesize 2D thin film with intrinsic defects to create pathways for the movement of metal ions to form filaments. **Figure 1**a shows the working principles of the MBE system, which utilizes heated pure solid sources of selenium and hafnium to generate atom beam fluxes that are then deposited onto the substrate surface during synthesis, enabling 2-inch wafer-scale material growth with precise control of the beam flux and substrate temperature. Details of the growth parameters of $HfSe_2$ synthesis are described in Section 4. Compared to CVD, where complex precursors are frequently used, our system can effectively eliminate the occurrence of by-products and impurities. Furthermore, the stable and well-controlled beam flux and the rotational substrate with uniform temperature distribution make it suitable for uniform wafer-scale $HfSe_2$ growth.

Figure 1b shows the in situ reflective high energy diffraction (RHEED) patterns measured during $HfSe_2$ growth at different growth times to monitor the growth of $HfSe_2/SiO_2$. As shown, the RHEED pattern taken before the growth (0 min; the top image) shows a typical RHEED pattern for amorphous SiO_2 substrate.[36] After 5 min of growth, the feature-less amorphous RHEED pattern evolves into streaky diffraction patterns, indicating a polycrystalline lattice structure.[37] The parallel streaks become sharper and brighter without Debye rings when the growth time exceeds 10 min, indicating a flat film without onset islands.[35] The pixel intensity line profiles along the dashed line as highlighted in the bottom image (10 min) are extracted and shown in Figure 1c, where an apparent increase of the streak brightness is found as the growth time is increased. The full width at half maximum (FWHM) of the zero-order streak is also extracted and shown in the inset of Figure 1c, revealing an evident decrease of FWHM. The streak brightness and FWHM trends confirm the improvement of crystallinity with thickness, which was also reported in epitaxy growth method.[38] Furthermore, the in-plane orientation of $HfSe_2$ during growth is analyzed by utilizing an azimuthal RHEED method, where the reciprocal space along different directions is measured by varying the azimuthal angle of the sample.[39] Figure 1d shows the azimuthal angle-dependent intensity profile (along the dashed line in Figure 1b) in a polar coordinate system, where the radius represents the reciprocal distance from the zero-order spot and the polar angle refers to the azimuthal angle. For material with preferred in-plane crystal orientations, the reciprocal space should exhibit discrete spots, indicating different RHEED patterns along with different azimuthal angles.[39] However, instead of showing discrete spots, a green circle (highlighted by the white dashed line) is observed in Figure 1d, which refers to the first order streak, indicating that the grains are randomized without any preferred in-plane orientation.[40] It is worth noting that such randomized in-plane grains are consistent with the substrate structure since the amorphous SiO_2 does not exhibit any crystal orientation. The RHEED analysis results reveal that a flat polycrystalline film is grown with its grains exhibiting no preferred in-plane orientation, indicating the existence of randomized grains and grain boundaries with intrinsic defects.

Ex situ characterization is performed to further understand the physical and chemical properties of the as-grown $HfSe_2$ film (Figure 1e). The growth rate is analyzed by measuring the film thickness with different growth times, showing a well-controlled growth rate of ≈1 nm min^{-1} (Figure S1, Supporting Information). Furthermore, a slight variation in thickness is measured at different positions across the 2-inch wafer for each growth time, indicating a uniform growth. Figure 1f shows the Raman spectrum with a clear A_{1g} peak at 199 cm^{-1}, and the X-ray diffraction (XRD) result proves the existence of strong (001) texture in $HfSe_2$ (Figure S2, Supporting Information), confirming the formation of a layered structure in $HfSe_2$

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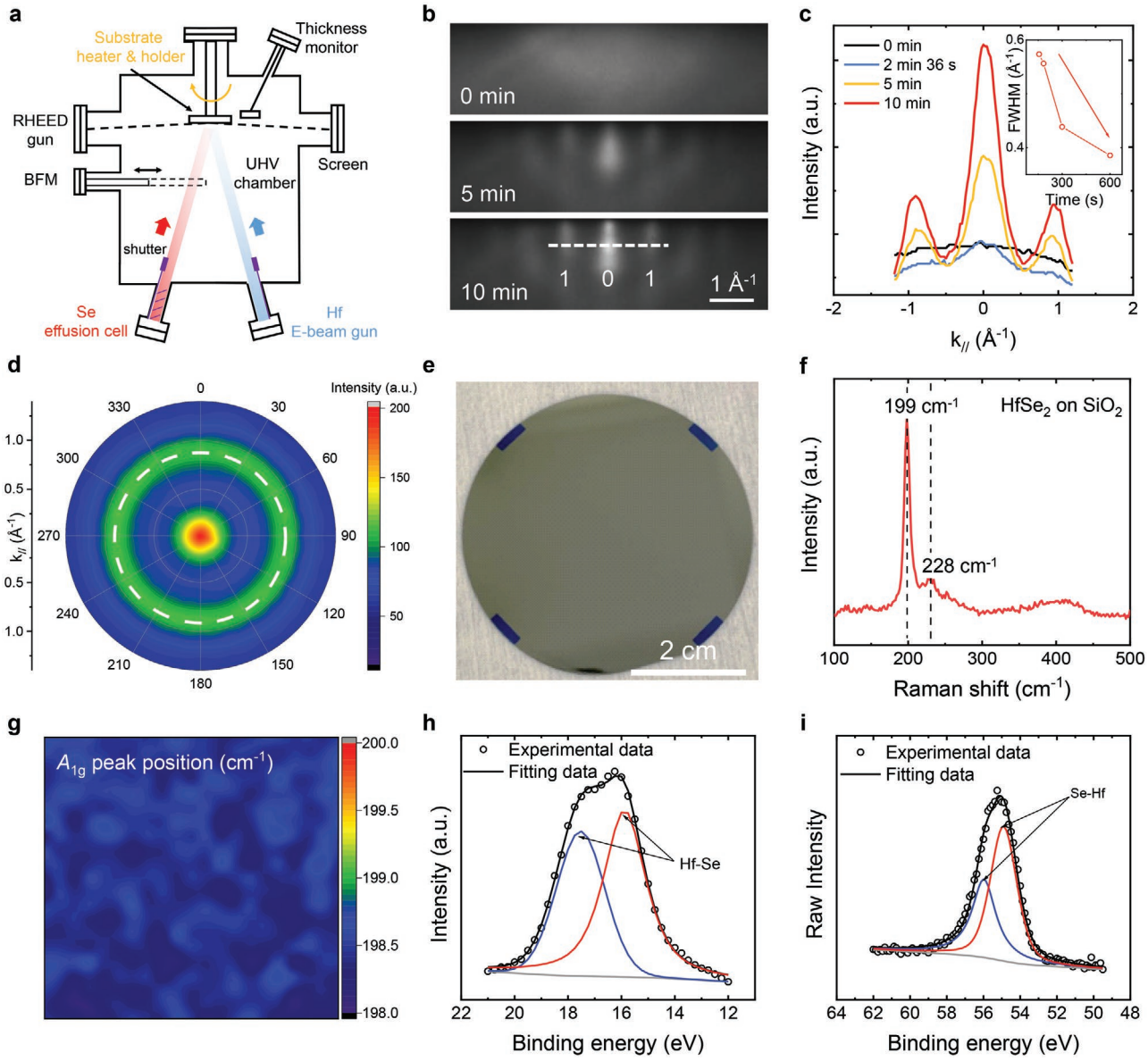

Figure 1. Growth and material characterization of the wafer-scale MBE-grown $HfSe_2$ thin film. a) An illustration of the arrangement of the substrate holder, Se and Hf flux. The Se flux and Hf flux are measured by beam flux monitor (BFM) and thickness monitor, respectively. b) RHEED patterns during growth. The white dashed line highlights the line scan region used in (c) and (d). c) The streak intensity line profile during growth. Inset shows the FWHM of the middle streak. d) The azimuthal angle-dependent intensity profile after growth. The white dashed circle highlights the first-order streak. e) Optical image of an as-grown $HfSe_2$ thin film on a 2-inch SiO_2/Si wafer. f) Raman spectrum of as-grown $HfSe_2$ thin film. g) Raman mapping of A_{1g} peak position over a 10 μm × 10 μm region. h) Hf 4f and i) Se 3d XPS peaks. The black arrows label the binding between Hf and Se.

film that is in good agreement with previous reports.[33,35,41] The uniformity of the $HfSe_2$ is further illustrated by the Raman mapping of the A_{1g} peak as shown in Figure 1g, where the color refers to the peak position value. In addition, Raman mapping of A_{1g} peak at five locations over the whole 2-inch wafer is shown in Figure S3, Supporting Information, which further confirms the uniformity of the as-grown $HfSe_2$ film. The details of Raman sample preparation and Raman mapping setup are discussed in Section 4. X-ray photoelectron spectroscopy (XPS) is also performed to confirm the chemical composition and elements directly, and the results are shown in Figure 1h,i. The binding energies of Hf 4f and Se 3d indicate the existence of chemical bonds between Hf and Se, which are also consistent with the previous report.[42] The fitted peak positions are listed in Table S1, Supporting Information. Based on the crystallinity analysis and material characterizations, uniform polycrystalline $HfSe_2$ growth is demonstrated on a wafer-scale substrate.

2.2. Metal-Assisted Van der Waals Transfer of Hafnium Diselenide

A wet process using chemical etchant (i.e., sodium hydroxide solution) is the most frequently used approach to transfer 2D

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film from as-grown substrate to the target substrate.[43] However, this process is usually followed by a deionized water rinse step to remove the solvent residuals, which introduces water molecules to the surface of 2D material, resulting in wrinkles and bubbles between the target substrate and 2D material.[44,45] Furthermore, external mechanical supporting layers, such as, polymethyl-methacrylate (PMMA), are necessary to prevent the film from cracking. However, these flexible organic polymers are difficult to clean thoroughly, especially after a long baking step, which is usually used to improve the adhesion of 2D material with target substrates.[44] To address these issues, we developed a metal-assisted vdW transfer method that avoids any wet process and direct contact between $HfSe_2$ and supporting layers. **Figure 2** shows the transfer steps and the associated fabrication process of the $HfSe_2$-based CBA. First, a layer of gold (Au) is deposited over the as-grown polycrystalline $HfSe_2$ (Figure 2a,b) and followed by the deposition of PMMA and adhesive tape as supporting layers (Figure 2c). It is worth noting that the Au capping layer not only prevents $HfSe_2$ from oxidation but also eliminates residuals and impurities at the interface between the $HfSe_2$ and Au layers. Moreover, $HfSe_2$ film can be directly peeled off from SiO_2 due to its strong interaction with Au layer (Figure 2d), thus resulting in a dry and clean process.[46,47] After the peel-off step, the film is pressed on the target substrate immediately and followed by heating using hotplate and acetone cleaning steps to release the adhesive tape and PMMA layer (Figure 2e–g). Then, top electrodes (TE) are patterned and deposited, and the remaining gold layer is etched away using reactive ion etching (RIE) (Figure 2h). Details of process parameters are shown in Section 4.

Figure 2i shows a microscope image of the fabricated CBA, and the highlighted square depicts the material stack in the crosspoint region where titanium (Ti) and Au are used as the bottom and top contact electrodes, respectively. Other CBA images with different array sizes are shown in Figure S4, Supporting Information. In other gold-assisted exfoliation processes, the Au layer needs to be fully etched away using solution etchant.[46] However, the Au capping layer remains at the crosspoint region using our approach, which can protect HfSe2 during the plasma etching step while serving as contact TE (Figure S5, Supporting Information). Figure 2j shows the surface roughness of the $Au/HfSe_2$ before and after transfer, indicating negligible effect on the film roughness by utilizing the metal-assisted vdW transfer technique. The insets show the optical images before and after transfer, showing the wafer-scale device fabrication capability that is suitable for realizing large CBA. Besides, microscope images and atomic force microscope (AFM) height images of the transferred $Au/HfSe_2$ stack film are shown in FigureS S6 and S7, Supporting Information, respectively, showing a flat and continuous transferred film with much less wrinkle density over a large area as compared to the hexagonal boron nitride (hBN) CBA,[14] which enables CBA with small device variation.

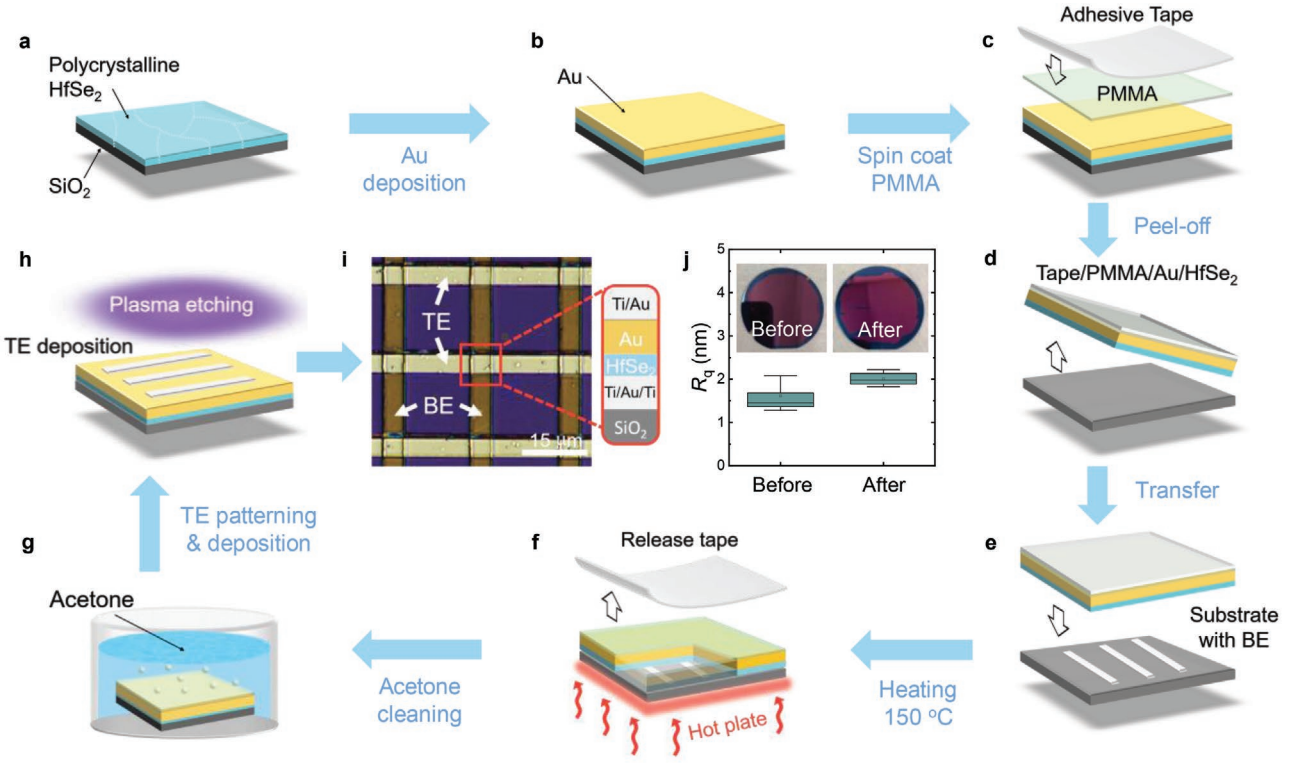

Figure 2. Schematic showing the metal-assisted vdW transfer technique and device fabrication process flow. a) As-grown $HfSe_2$ thin film. b) Au layer deposition. c) PMMA spin coating and adhesive tape cover. d) Peel off $HfSe_2$. e) Transfer to the target substrate. f) Heat up and release tape. g) Acetone cleaning and remove PMMA. h) Top electrode deposition and Au dry etch. i) Optical microscope image of a CBA. The right inset highlights the material stack at the cross point region. j) Surface roughness of $Au/HfSe_2$ film before and after transfer. Insets show the optical image of the large-scale vdW transfer.

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2.3. Direct Current Characterization and Switching Mechanism of Hafnium Diselenide Memristor

2.3.1. Direct Current Characterization of Hafnium Diselenide Memristor

Figure 3a shows a typical RS *I–V* curve of our memristors, and the black arrows label the voltage sweep order. The voltage is defined as the potential difference between the Ti electrode (V_{Ti}) and the Au electrode (V_{Au}), leading to an electric field from Ti to Au under positive voltage bias and vice versa. The device switches from high resistance state (HRS) to low resistance state (LRS) under positive voltage sweep and remains at LRS even when the voltage passed through 0 V to negative bias, showing a typical nonvolatile RS property. A positive voltage sweep is required for SET (transition from HRS to LRS), whereas a negative voltage sweep is needed for RESET (transition from LRS to HRS), indicating a typical bipolar characteristic similar to other conductive-bridge memristors.[15,48,49] During the SET process, a small set voltage (V_{set}) is extracted at around 0.6 V, showing a low operation voltage than other 2D material-based memristors.[15,18,19,23,50,51] Moreover, a low power consumption of only 0.82 pJ is needed to set the device (Figure S8, Supporting Information), manifesting its suitability

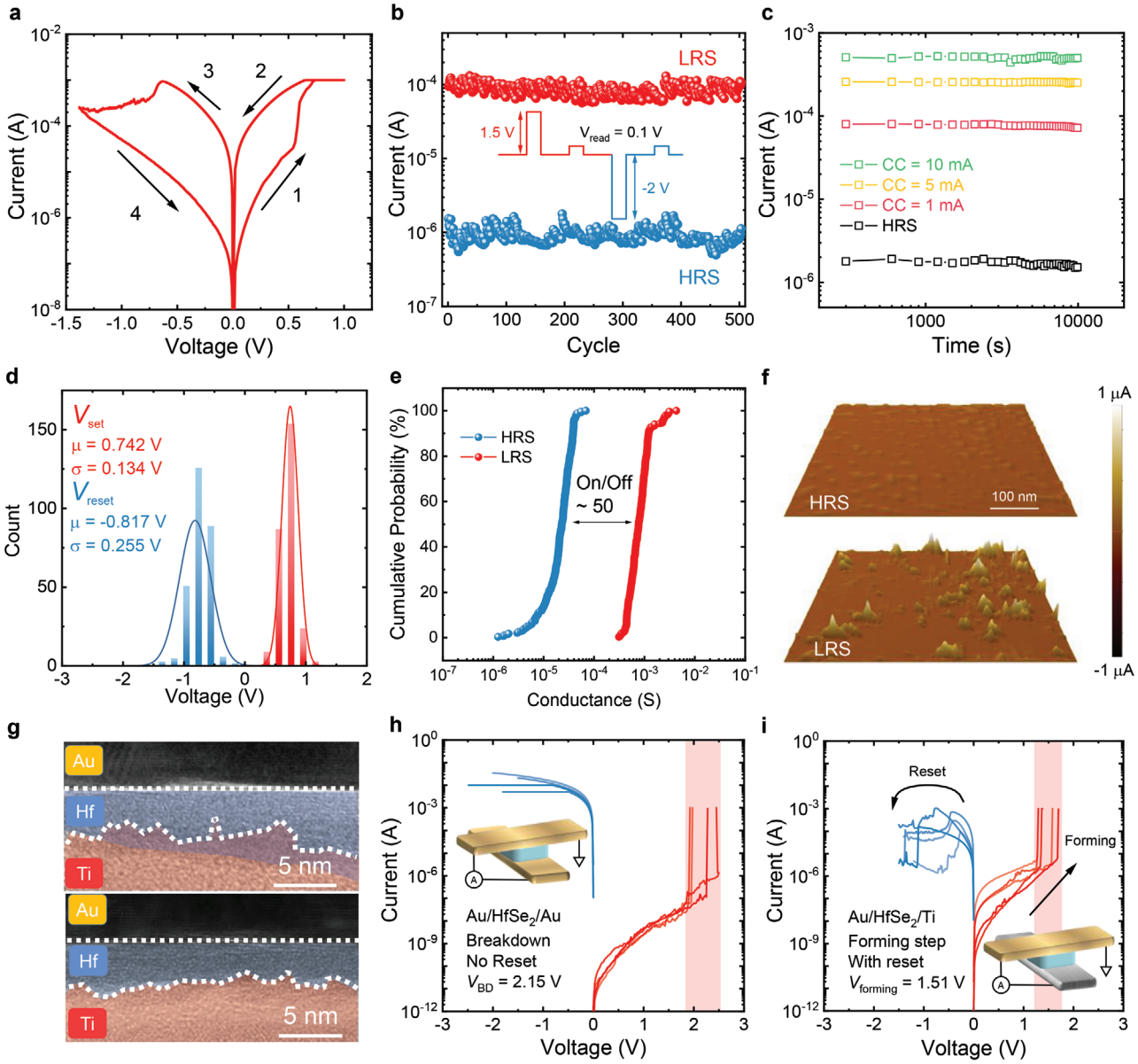

Figure 3. DC characteristics and the RS mechanism. a) A typical RS *I–V* curve of a memristor. The black arrows label the voltage sweep order. b) The endurance test of 500 cycles. The inset shows the voltage scheme for set and reset steps. c) Retention test of multiple conductance states under different compliance currents. d) V_{set} and V_{reset} distribution among 38 different devices. e) Cumulative probability of both HRS and LRS conductance value. f) C-AFM conductance map of HRS and LRS. g) Cross-sectional TEM images at regions with and without Ti filaments. h) Hard breakdown process of the Au/$HfSe_2$/Au devices. i) Electroforming step and the reset process of the Au/$HfSe_2$/Ti devices.

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for energy-efficient applications. To further evaluate the performance of such devices as memristors, endurance, retention, and statistical analysis are carried out. An endurance test exhibiting a RS ratio of ≈100 for a cycle number of more than 500 is obtained and shown in Figure 3b, indicating the stability of such devices during cycle-to-cycle measurement. The inset shows the voltage supply scheme during the measurement, where the HRS and LRS are constantly measured and extracted at +0.1 V. Moreover, the retention results with multiple resistance states are shown in Figure 3c, and a retention time of longer than 10^4 s is demonstrated for all four resistance states, indicating a stable nonvolatile characteristic with multiple conductance tunability. The different LRS shown in Figure 3c is obtained using different compliance currents, and the similar HRS values in different cycles are adjusted by different negative voltage sweep range (see Figure S9, Supporting Information, for detailed *I*–*V* curves). Furthermore, a statistical analysis of V_{set}, reset voltage (V_{reset}), conductance of HRS and LRS are shown in Figure 3d,e, showing a comparable device variation to other 2D material-based memristors.[52] In Figure 3d, an average V_{set} of ≈0.7 V is measured, leading to a low power consumption. Figure 3e shows the cumulative probability distribution of HRS and LRS, and a RS ratio of ≈50 times is retained despite experiencing a spatial variation.

2.3.2. Resistive Switching Mechanism

The electrochemical metallization mechanism is one of the most frequently used explanations for 2D material-based memristors, where the conductive filament is formed by active metal ions driven by external bias, such as Ti, Ag, Cu.[12,15,53] In a similar fashion, we reveal that the RS mechanism is based on the formation and rupture of metallic filaments. To verify that the RS is taking place at localized regions (i.e., filament), conductive-atomic force microscopy (C-AFM) confirms the formation of conductive filaments at LRS as compared to the conductance map of HRS (Figure 3f). The details of C-AFM measurement are explained in Figure S11, Supporting Information. To verify the composition of conductive filaments in the switching medium, transmission electron microscopy (TEM) and energy dispersive X-ray (EDX) are performed, as shown in Figure 3g. The TEM image is re-colored based on the EDX results (Figure S12, Supporting Information), and the white dashed lines highlight the region of Au and Ti. The apparent overlap region between Ti and $HfSe_2$ is found in the top image compared to the bottom image, indicating the diffusion of Ti inside the switching medium, which results in the formation of conductive filaments. The atomic percentage line profile of EDX is plotted in Figure S13, Supporting Information, which clearly shows a higher Ti atoms volume in the overlapped region than the other regions. To further confirm the switching mechanism, electrical measurements are carried out using Au/$HfSe_2$/Au device as the control sample. It should be noted that our devices possess the electroforming step, and the *I*–*V* curves of the forming step between the memristors and control samples are compared. Figure 3h shows the first time "electroforming step" and the successive negative voltage sweep among four control samples. The device is unable to reset back to HRS after a positive voltage sweep, indicating the occurrence of a hard breakdown (BD) instead of soft breakdown (or electroforming), with an average BD voltage (V_{BD}) of 2.15 V. On the contrary, in Figure 3i, the devices can be reset back to HRS, and the average forming voltage ($V_{forming}$) is 1.51 V, which is less than 2.15 V in control samples, implying that the RS is strongly dependent on the Ti electrodes. Besides, the smaller $V_{forming}$ compared to V_{BD} is attributed to the diffusion of Ti that facilitates the forming step in Au/$HfSe_2$/Ti sample, which is consistent with other memristors that are also relying on active metal filaments.[14] In addition, Figure S14, Supporting Information, shows the C-AFM current maps of the electroformed and BD samples. A large conductive region is found in the Au/$HfSe_2$/Au sample after BD, which may be caused by the irreversible structural deformation under high electric field stress.[54] However, by forming at a lower bias, the Au/$HfSe_2$/Ti sample only shows localized conductive filaments, indicating that structural deformation is absent and thus the RS behavior is caused by the Ti-based filament mechanism. Besides, the defects in 2D materials also play an important role as active metal ion diffusion paths in the RS medium. For devices based on single-crystal material with negligible defects, such as, exfoliated hBN and epitaxial silicon (Si), the RS characteristic is inhibited due to the lack of defect-induced diffusion paths for filament formation.[15,48] However, the RS behavior occurs when defects or dislocations are introduced into these materials, in which a higher defect density is shown to reduce the forming voltage (Figure S16, Supporting Information).

2.4. Implementations of Hafnium Diselenide-Based Crossbar Array

2.4.1. Synaptic Plasticity and Modeled Artificial Neural Network

As one of the basic components in human brain, synapses are the direct neuron-to-neuron connection units where spikes generated by the pre-synaptic neuron are transmitted to the post-synaptic neuron by releasing neurotransmitters. Moreover, the strength of such connection can be refreshed based on the spikes, which is known as synaptic plasticity.[4] In this way, an artificial synapse can be mimicked using a two-terminal memristive device that possesses tunable conductance values. Here, we demonstrate an artificial synapse using $HfSe_2$-based memristor, where the Ti and Au electrodes are mimicking the pre-synaptic and post-synaptic terminals, respectively. Moreover, the current measured at a small read voltage (0.1 V) represents the post-synaptic current (PSC), often referring to the synaptic weight. **Figure 4**a shows long-term potentiation and depression (LTP and LTD) under identical positive and negative pulse trains. Pulse train with larger amplitude leads to more efficient control of the synaptic weight, indicating synaptic amplitude dependence plasticity (SADP). Such SADP is a vital behavior for biological synapses in responding to external chemical stimulations, which induce a change in action potential and influence synaptic plasticity.[55] To further investigate such behavior, another frequently used nonidentical pulse train with increasing pulse amplitude is applied to the device, and the modulation of stimulated synaptic weight is shown in Figure 4b.[56,57] The pulse amplitude varies from 0.6 to 0.85 V (−0.7 to −1.1 V) during potentiation (depression), and the device

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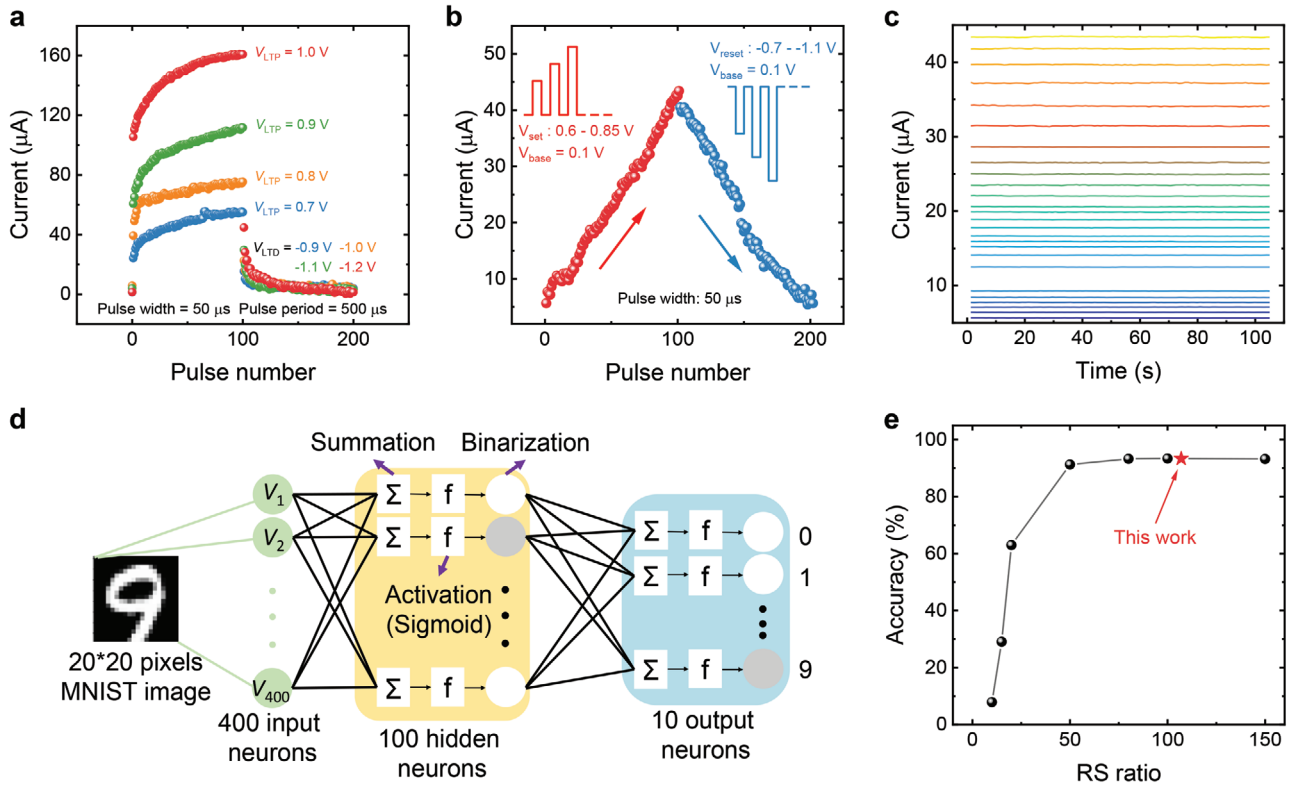

Figure 4. Artificial synapses and ANN implementation. a) LTP and LTD under positive and negative pulse trains with identical pulse amplitude. b) LTP and LTD under pulse train with nonidentical pulse amplitude. Insets show the waveform of the nonidentical pulses. c) Retention of 26 conductance states during the analog transition from HRS to LRS. d) Schematic of the fully connected ANN using $HfSe_2$-based synapse. e) Sensitivity of the recognition accuracy under different RS ratios. The highlighted point uses data measured by a pulse train with identical amplitude.

conductance is measured at 0.1 V. Pulses with small amplitude can slow down the initial change of PSC, whereas pulses with large amplitude can prevent the device from saturation, indicating the amplitude sensitivity of the devices. Besides, the retention results of 26 conductance states measured after every four pulses are shown in Figure 4c, indicating a typical analog transition of conductance states. To this end, a fully-connected perceptron neural network is simulated using the NeuroSim+ platform to perform offline classification based on the Modified National Institute of Standard and Technology (MNIST) database.[58] As schematically shown in Figure 4d, the ANN constitutes 20×20 input neurons, 100 hidden neurons, and 10 output neurons. The 400 input neurons correspond to the input black and white images with 20×20 pixels encoded from the MNIST dataset, and the pattern recognition results (0–9) are presented through the ten output neurons. The weighted sum is processed with sigmoid activation and binarization functions and then propagated to the output neuron layer.

During the simulation, the ANN is pre-trained by software using the training dataset of MNIST, and then the hardware is emulated to classify the MNIST testing dataset. Offline classification shows good tolerance to the linearity of LTP and LTD because the conductance value of each synapse can be iteratively programmed to the desired value.[59] In this way, although the measured LTP and LTD data may exhibit nonlinearity under identical pulse trains (Figure 4a), they are still applicable to offline classification. Moreover, identical pulse trains also reduce the time latency and power consumption of the periphery circuit.[57] In addition, the implementation of offline classification using other memristive CBA has been reported to evaluate the synaptic device performance under real-world scenarios.[5,60,61] A high recognition accuracy of 93.34% is achieved using the data measured at 1.0 and –1.2 V (Figure 4e). To prove the programming reliability of the device, we measured LTP and LTD consecutively to extract the cycle-to-cycle variation from Figure 4a (shown in Figure S17, Supporting Information). Here the variation is extracted in terms of the percentage of the current range (maximum current—minimum current). A small cycle-to-cycle variation of 2.42% is achieved as compared to other electronic synapses.[62] Moreover, the endurance test at 85 °C is also shown in Figure S18, Supporting Information, indicating the stability under harsh operating conditions.[52,63] The sensitivity of offline classification to RS ratio is also investigated. Figure 4e shows an apparent improvement in recognition accuracy with increasing RS ratio as it could compensate for the non-zero HRS leakage current.[60]

2.4.2. Accurate and Energy-Efficient Multiply-and-Accumulate Operation and Convolution Image Processing

MAC operation is a core computational operation for matrix-heavy applications such as pattern recognition, signal processing, and speech recognition.[5] As shown in **Figure 5**a, a

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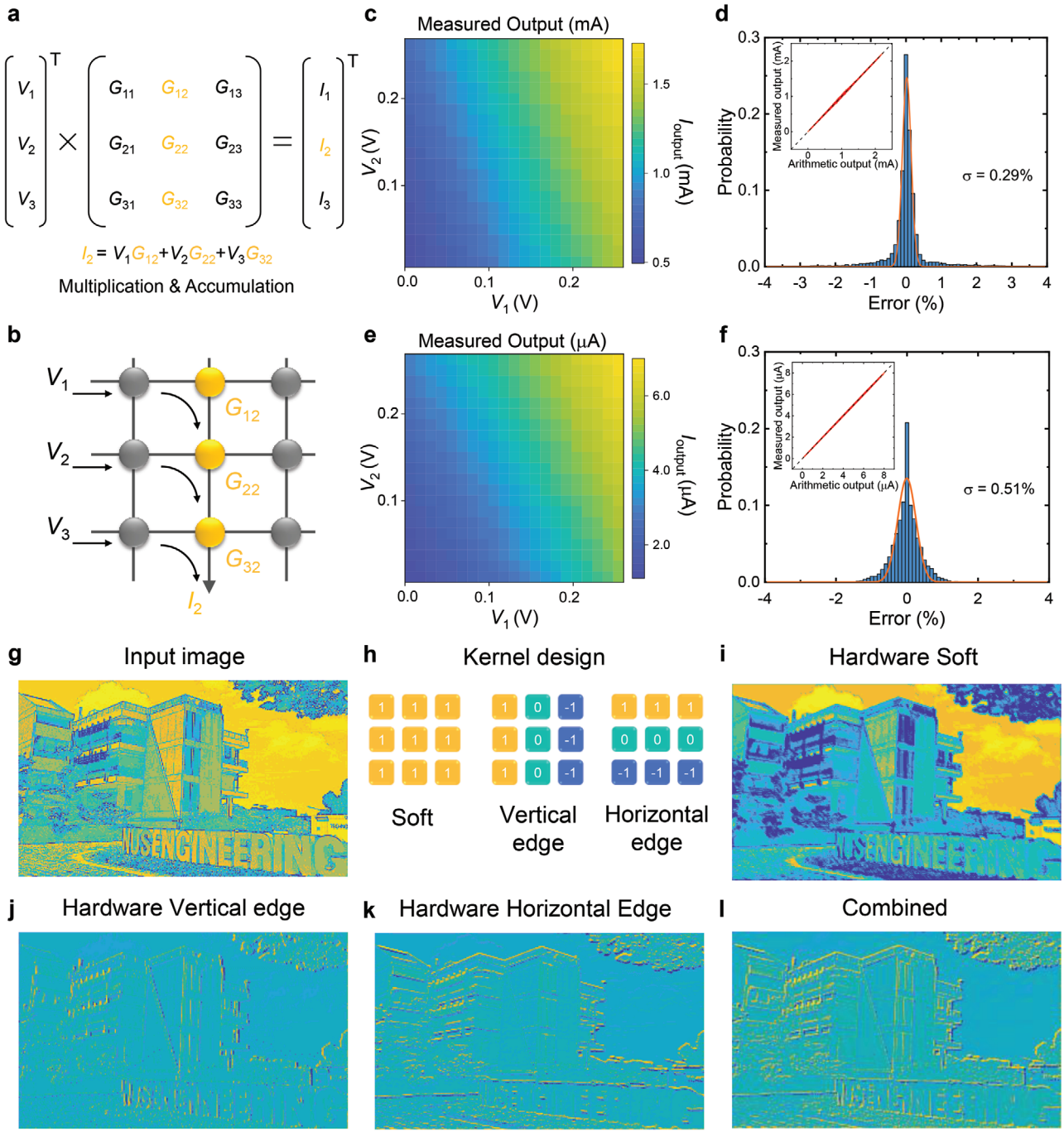

Figure 5. MAC and image processing implementations using $HfSe_2$ memristive CBA hardware. a) Mathematical expression of MAC operation. b) Schematic of hardware MAC operation between input voltage vector and device conductance matrix. The yellow-colored cells label the column that is being measured. c) Measured output current mapping under LRS condition. d) The corresponding distribution of error between measured and arithmetic results. The inset shows the relationship between the measured and arithmetic currents. e) Measured output current mapping under HRS condition. f) The corresponding distribution of error between measured and arithmetic results. The inset shows the relationship between the measured and arithmetic currents. g) The original input image. h) Different kernel designs. i–k) Processed images using hardware with different kernels, including soft, vertical, and horizontal edges. l) The combination of figure (j) and (k), showing edge detection in both directions.

vector-matrix multiplication (VMM) operation comprises an input vector, a matrix, and an output vector. Moreover, the output vector I_j follows the equation: $I_j = \Sigma_i V_i G_{ij}$, where V_i and G_{ij} refer to the input vector and the matrix values, respectively. For a M × N matrix, the entire VMM operation requires M × N number of multiplications and (M–1)× N number of additions, resulting in additional power consumption during the data movement in conventional von Neumann architecture.

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However, in memristive CBA structure, the input vectors and matrix values are physically connected, and the voltage-conductance multiplications and current-current additions are performed through Ohm's law and Kirchhoff's current law, respectively. As shown in Figure 5b, the vector-matrix network can be directly mapped into a CBA, where V_i refers to the input voltage vector, and I_j refers to the output current vector, resulting in a simplification of the number of operations and high degrees of parallelism by direct current measurement. Moreover, because of the programmable crosspoint conductance in the memristive CBA, it becomes convenient to refresh the matrix values to achieve different MAC operation-based applications using the same CBA.[5]

Here we consider a situation where three voltage inputs (V_1, V_2, V_3) come from three rows of memristors in the CBA, and the output vector I_j is measured column by column (as shown in Figure 5b). Figure 5c shows the measured output current mapping from one column when all the three devices are at LRS. During the measurement, V_1 and V_2 vary from 0 to 0.255 V, whereas V_3 is kept at 0.128 V, and the current increases monotonically with the input voltage, which is consistent with Ohm's law and Kirchhoff's law. Different current mappings under different V_3 are also measured and shown in Figure S19, Supporting Information, showing MAC operation with a variable input vector. The error between measured and arithmetic results is shown in Figure 5d, where a small error standard deviation of 0.29% is extracted in one column. After the memristors are reset to HRS, the output current mapping is measured and compared again, and an error standard deviation of 0.51% is achieved (Figure 5e,f), manifesting high-accuracy MAC operations. Insets in Figure 5d,f show the relation between the measured current and the arithmetic current with a narrow distribution and slope close to 1, indicating good consistency between the measured and expected output current. Moreover, the power efficiency of the CBA for MAC operation is estimated to be around 8-trillion operations per second per Watt, showing the potential for energy-efficient computing hardware (Table S2, Supporting Information).

Convolution neural network is a practical hardware implementation that utilizes the MAC operation to enable efficient feature extraction of images via convolutional image processing.[64] Figure S21, Supporting Information, shows the detailed procedure of hardware-based convolutional image processing. The input voltage signals are mapped from the pixel values of the original images. For each pixel of the original image (Figure 5g), a convolution operation is carried out among the local neighboring voltage values (9 voltage inputs in total) and the programmed 3×3 conductance matrix. During the convolution operation, the MAC operations in the same column are performed by directly measuring the output current. The output current from each column is added together arithmetically, resulting in the final output current (I_{out}) at a specific pixel position (P_{ij}). Finally, the output current map is reorganized and plotted as the output processed image.

Figure 5h shows the convolutional image processing using three different kernels, including soft, vertical edge detection, and horizontal edge detection. As for the actual kernel programming, the conductance matrix is mapped from a 3×3 convolution matrix, and the sign of each conductance matrix element is determined by the conductance difference between HRS and LRS (Figure S21c, Supporting Information).[5,49] During this step, we program the kernel values based on the difference between the conductance of HRS and LRS of each memristor in the CBA, taking into account the device-to-device variation. The detailed designs of the equivalent conductance matrix for all three kernels are shown in Figure S22a, Supporting Information. The hardware processed images are shown in Figure 5i–l. As depicted in Figure 5i, the soft filter leads to a blurred image because it takes the average at each pixel position based on the surrounding pixel values. In Figure 5j,k, the different edge detection results originate from the kernel directions, in which the finite difference calculation at the local region is performed along with different directions, which are also essential filtering functions frequently used in image processing. The detailed processing method of Figure 5l is described in Figure S22b, Supporting Information, showing edge detection at both horizontal and vertical directions simultaneously. The comparison between software and hardware processed images is presented in Figure S23, Supporting Information. In software processing, the kernel values are designed accurately under a device-variation-free condition, but such device variation is considered in hardware processing. We show that both software and hardware processed images achieve similar results, indicating that the CBA is tolerant of device variation and capable of performing convolutional image processing based on MAC operation. Nevertheless, such device variation is also found in other CBAs, but the hardware processed images still achieve a high level of similarity to the software processed images.[61,65] This implies that the image processing results are not severely influenced by device variation in a small CBA. However, for MAC operations in a large-scale array, the device variation, sneak current, and current-resistance (IR) drop issues would have a more profound influence on the computing accuracy.[5] Therefore, further optimizations of material growth such as doping and thickness modulation could be explored to improve the device variation.[14,22,66] In addition, integration with access transistors or selectors is necessary to improve the computing accuracy in large-scale arrays,[5,67–69] which will be investigated in future work.

3. Conclusion

We have demonstrated a practical approach to implement memristor CBA in neural network hardware based on wafer-scale polycrystalline $HfSe_2$ thin film. A metal-assisted vdW transfer technique is developed to enable large-scale $HfSe_2$ film transfer, which serves as a universal platform to integrate other 2D materials in memristor CBAs. The memristors exhibit small switching voltage, stable endurance, and retention, as well as, low switching energy, indicating a stable control of conductive filaments via the defect paths in the polycrystalline film. Moreover, the CBA successfully implements both neuromorphic and matrix-heavy workloads in neural networks, including artificial-synapse-based ANN, energy-efficient MAC operations, and convolutional image processing. Notably, high recognition accuracy is achieved in ANN, revealing its potential for neuromorphic computing. Moreover, the column-by-column MAC

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operation manifests a highly parallelized computing operation, opening a route to emerging applications in hardware accelerators for matrix-heavy workloads related to artificial intelligence (AI) and machine learning.

4. Experimental Section

Hafnium Diselenide Synthesis Using Molecular Beam Epitaxy: $HfSe_2$ was deposited on a commercially purchased p-type 2-inch silicon wafer with 100 nm SiO_2 (University Wafer) in an ultra-high vacuum MBE system (Eiko EW-100S). Pure solid Se (99.999%, Furuuchi Chemical) was placed in a k-cell and the Hf (99.9%, Furuuchi Chemical) source was placed in a carbon crucible faced to the electron beam gun.

The detailed process flow was as follow: The substrate was first heated to 800 °C over 60 min and maintained for 10 min for degassing purpose, and the Se cell was heated to around 145 °C with a flux of 2×10^{-6} Torr during the same period. The substrate temperature was then decreased to 750 °C over 15 min and maintained for growth. Afterward, the electron beam gun intensity was increased to 100 mA with a Hf flux speed of 0.05 Å s^{-1}. Next, the shutters of substrate, Hf electron beam gun, and Se k-cell were open and maintained for 5–30 min, depending on the required thickness. The substrate was kept rotating during the entire process, and the chamber pressure was maintained below 10^{-8} Torr.

Hafnium Diselenide Material Characterization: The $HfSe_2$ was characterized by Raman spectroscopy (Renishaw, inVia), XPS (Quantera PHI II), TEM, and EDX (Talos F200X). A 30 nm thick $HfSe_2$ film was used for Raman single spectrum and mapping (Figure 1f,g) to minimize the laser oxidation effect to the Raman peaks of $HfSe_2$.[30,35] During the Raman spectrum, the laser power was limited by a small filter of 1% to reduce the laser oxidation. The Raman mapping was taken at a 10 μm × 10 μm region, with a step of 0.5 μm.

Device Fabrication: First, a 15 nm gold layer was deposited over the as-grown $HfSe_2$ thin film by E-beam evaporation (AJA E-beam evaporator). Second, two layers of PMMA 495 A4 were spin-coated over the Au layer with 1000 and 4000 rpm, respectively. After each spin coating, the coated PMMA was heated at 180 °C for 2 min. A layer of adhesive tape (SPS 1007R-13.0) was then pressed over the baked PMMA. Third, the Au/$HfSe_2$ stack was peeled off and transferred to the target substrate. The bottom electrodes on the target substrate were fabricated by a Laser Writer patterning process (Hiedelberg DWL66+) followed by a Ti/Au/Ti (10/30/20 nm) metal deposition process and lift-off process. Afterward, the target substrate was heated at 100 °C for 5 min to enhance the adhesion, and was then heated to 150 °C for 3 min to release the tape. The remained PMMA layer was resolved and cleaned with acetone for 1 h. The top electrodes were then fabricated by another patterning process followed by Ti/Au (20/40 nm) deposition and lift-off process. Finally, the middle Au film was etched away by SF_6 -based RIE (Oxford ICP Etch Cluster) technique to form the crosspoint CBA.

Electrical Characterization: All DC *I–V* characteristics were measured using a Cascade probe station with an HP4155B semiconductor parameter analyzer. The input and output of VMM were also supplied and measured by the HP4155B analyzer. Synaptic pulse measurements were performed by Tektronics S4200 semiconductor parameter analyzer. The high-temperature measurement was performed by Lakeshore cryogenic probe station. All room temperature electrical measurements were carried out in the ambient condition. The endurance at 85 °C was measured in the vacuum condition.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D hafnium diselenide, image processing, multiply-and-accumulate operation, neural network hardware, van der Waals transfer

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